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44.5 GHz PHEMT POWER AMPLIFIER

by

Scott McLelland, Malcolm G. Stubbs and Gilbert A. Morin

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Scott McLelland
Carleton University

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Malcolm G. Stubbs
Communications Research Centre

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Gilbert A. Morin
SST/MILSATCOM
Defence Research Establishment Ottawa

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Abstract

The work described in this report represents the design phase of a gallium arsenide monolithic microwave integrated circuit (GaAs MMIC) power amplifier using pseudomorphic high electron mobility transistors (PHEMTs). The main purpose was to investigate the possible performance of a power amplifier at 44 GHz for future application in a phased array antenna system. The design of a two stage amplifier, providing over 12 dB of gain over the frequency range 43.5 - 45.5 GHz, is described along with the expected large signal performance. It is expected that the amplifier will provide over 20 dBm of output power. The final layout of the complete chip is also presented.

Résumé

Ce projet décris les étapes de conceptions d'un amplificateur de puissance utilisant la technologie de fabrication de circuit monolithic sur l'Arsenure de Gallium (GaAs MMIC) avec des transistors à effet de champ à hétérostructure pseudomorphic (PHEMT). Le but principale était de déterminer les performances réalisable d'un amplificateur de puissance à 44 GHz qui pourrait ensuite être utilisé comme composante d'une antenne réseau. La conception d'un amplificateur à deux étages, fournissant plus de 12 dB de gain de 43.5 à 45.5 GHz, est décris avec les résultats de simulation non-lineaire. Il est prévue que l'amplificateur fournisse au delà de 20 dBm de puissance de sortie. Le plan final du circuit est aussi présenté.

Executive Summary

The design procedure for a 44.5 GHz, gallium arsenide monolithic microwave integrated circuit (GaAs MMIC) power amplifier is presented. This report outlines the initial determination of the appropriate transistor size and its bias conditions in order to meet the amplifier specifications. Non-linear design techniques, used to predict the performance of the amplifier at its maximum power level of operation, are also introduced. Input and output matching networks are developed and the predicted amplifier performance, including associated bias networks, is presented. The final amplifier layout is shown and the amplifier performance predictions are confirmed through the use of an electromagnetic simulation design tool. Finally the amplifier is shown to be cascadable allowing sufficient gain to be achieved for a driver stage application. The amplifier will be fabricated at the Northrop Grumman foundry and will be measured in January 1998.

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List of Figures and Tables

I. Specifications

This project was an investigation to determine potential GaAs MMIC amplifier performance around 44 GHz using the Northrop Grumman foundry power process, A detailed amplifier specification was not available and target specifications were used to guide the investigation as follows:

Frequency range	43.5 - 45.5 GHz
Power output	100 mW
Gain	> 10 dB
Return loss	> 10 dB on both ports
Size	3 x 2 mm maximum

II. Design

The design process is outlined in the following sections.

A. Amplifier Topology

The amplifier was to be operated in a conventional common source configuration. The device operating point was first chosen and then the performance of various device sizes were compared using small and large signal analyses. The results of this comparison were used to select the device size and number of stages required.

DC Bias

Class A quiescent operation was chosen for linearity and simplicity. The Northrop Grumman Design Manual (hereafter 'the design manual') suggested a typical Class A operating point of 50% I_{DSS}, $V_{GS} = -0.5$ V and $V_{DS} = 5$ V and hence this was chosen as the dc operating point. Simulated I-V curves for a 300 μm device are shown in Figure 1.

Small Signal Analysis

Small signal analysis was used to compare device sizes on the basis of gain, input/output impedance and stability. Since small signal S-parameters and maximum available gain (MAG) define the best achievable parameters they were used to compare device sizes. The MAG, S-parameters and stability of various devices is given in Figures 2, 3 and 4 respectively.
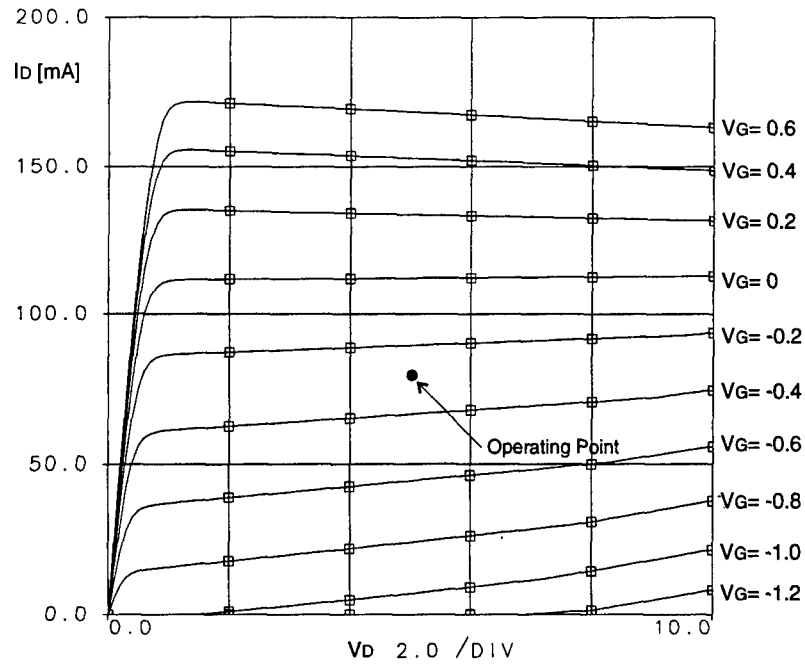
1

Figure 1: Simulated I-V curves for a 300 µm Northrop Grumman PHEMT.

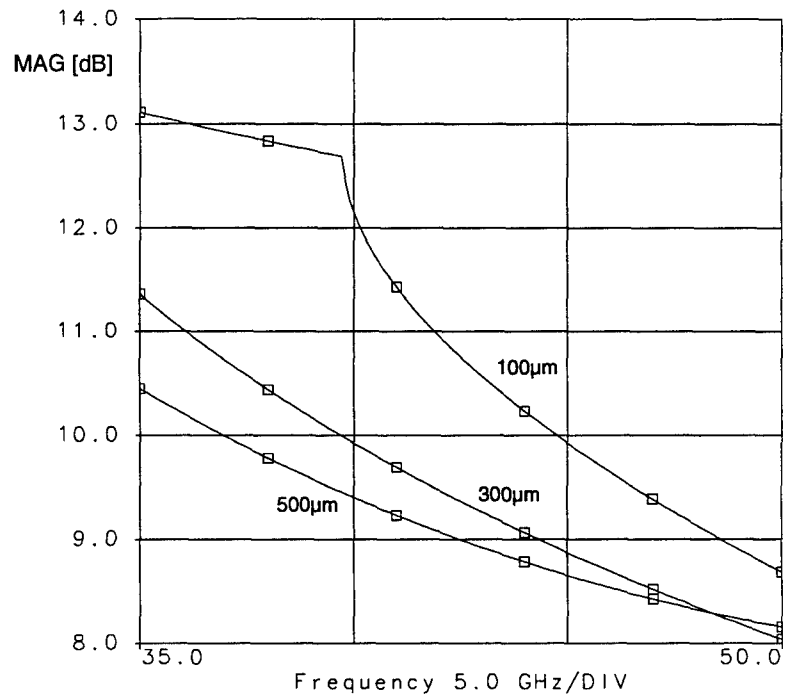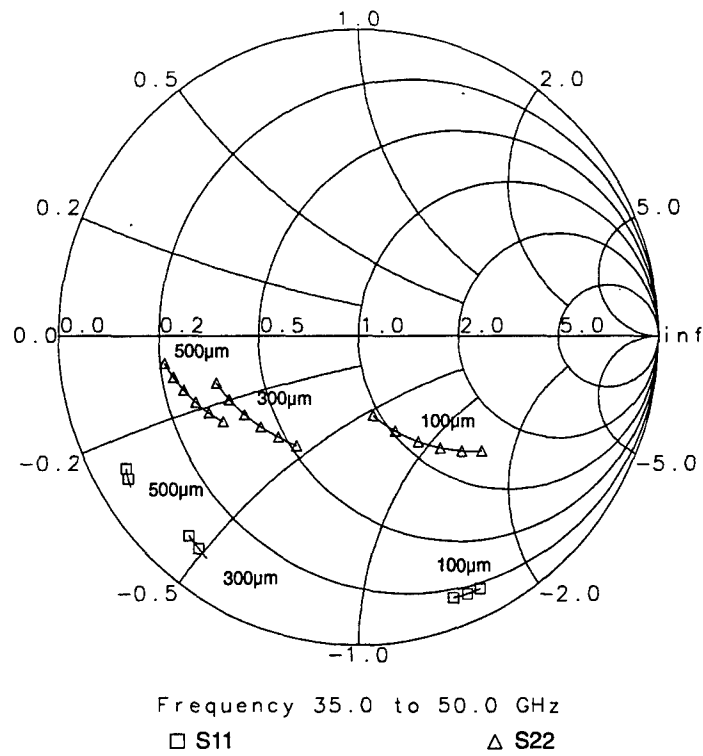**Figure 2: Maximum available gain for various device sizes.**

Figure 3: Input and output impedance plots for various device sizes.

Frequency 35.0 to 50.0 GHz

□ S11   △ S22
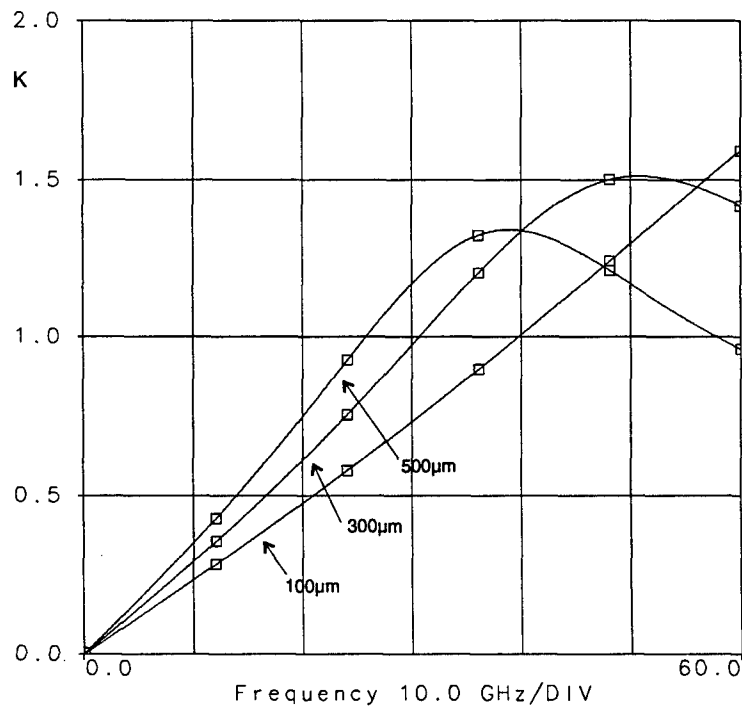
Figure 4: Small signal stability for various device sizes.

A preliminary device size of 300 µm was chosen. The design manual provided an approximation of 0.5 W per mm of device gatewidth. It follows that the 300 µm size should give approximately 21.8 dBm of output power and hence meet the design specification of 20 dBm with some margin. Further, Figure 2 shows that the 300 µm device could provide approximately 9 dB gain and Figure 3 shows that the input and output impedances are well behaved, varying relatively slowly with frequency. Finally, according to Figure 4, the 300 µm device shows instability below approximately 30 GHz (since K<1). However, preliminary analysis indicated that this should be correctable by adding stabilizing resistors behind the chokes since the instability was not in the band of interest.

Large Signal Analysis

The device was then evaluated for large signal performance since the design manual only approximated the output power. A load pull analysis was used to find the maximum output power and the associated optimum power load. The design manual provided an approximate optimum power load at 10 GHz that was scaled to a centre frequency of 44.5 GHz. The device was terminated by this approximate optimum load for power and the input was conjugately matched. The output power, as a function of input power, was then simulated using Harmonic Balance techniques, from which the 1 dB compression point was found to be 12 dBm. Using this 1 dB compression point as the approximate input power to the device, a load pull analysis was performed and the results are shown in Figure 5.

The load pull analysis confirmed that the 300 µm device should meet the performance requirement with an output power of 20.2 dBm given an optimum normalized load of 0.3+j0.2 Ω. The output power of the device was also considered for the case of the output conjugately matched with a normalized load of 0.18+0.29 Ω. The results are shown in Figure 6, and it is clear that the optimum load provided more output power. However, the small signal gain is only slightly less than the conjugately matched case. This was expected since the optimum load for power is very close to the conjugately matched load.

Given these results the amplifier was matched for optimum power. The amplifier could also be used as a driver since the small signal gain is not significantly smaller than for the conjugately matched load.

□ Output Power at 44.5 GHz [dBm]
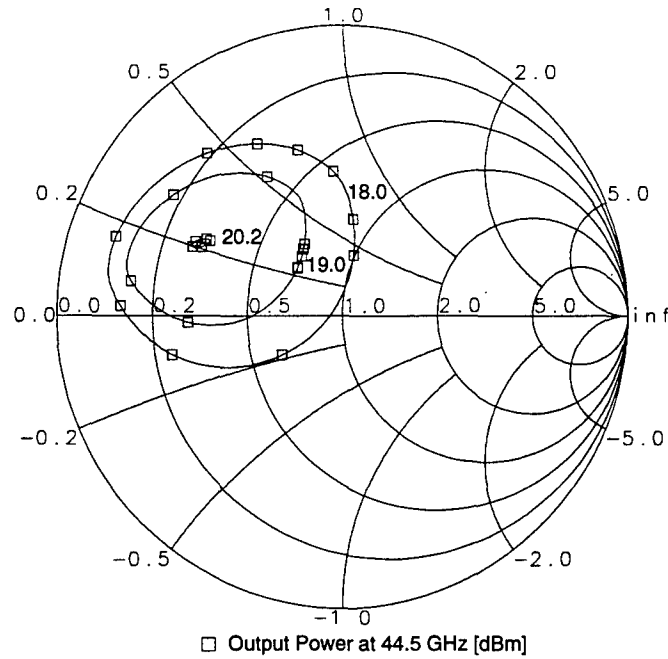
Figure 5: Load pull contours of 300 μm device (12 dBm input power).

M1 Power=12.0000000 value=20.2104400
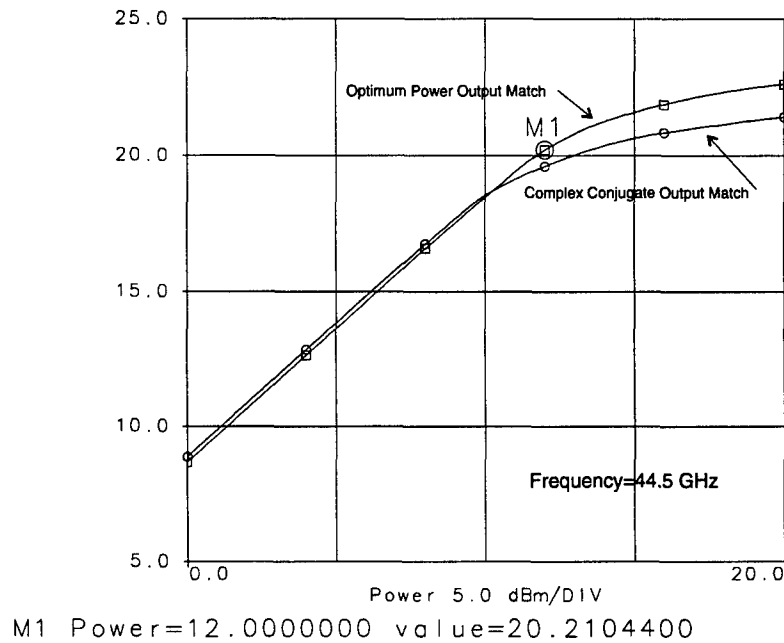
Figure 6: Comparison of output power for optimum power load and conjugately matched load for a 300 μm device.

All of the aforementioned analysis was performed at the Class A bias point of 5V on the drain. It was required to investigate if 3V on the drain could achieve the same performance at an increased level of efficiency. Therefore the entire large signal analysis was performed with 3V on the drain. Note that in this case the design manual approximate optimum load

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was scaled according to frequency and bias. The resulting load pull contour is shown in Figure 7.
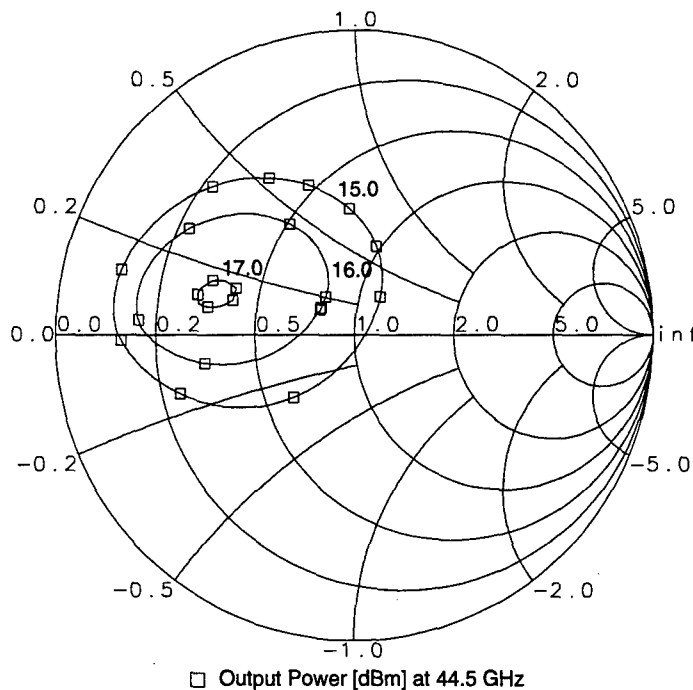
Figure 7: Load pull simulation of a single 300 μm device with 3V drain bias.

From Figure 7 the maximum output was 17 dBm and was not sufficient to meet the requirements and hence, a drain bias of 5V was selected. Clearly, in order to increase the efficiency another topology such as Class B or C must be used. However, Class A was chosen for simplicity.

In summary, a 300 μm device was selected achieving a gain of up to 9 dBm and 20 dBm output power. With the gain known, two stages were selected such that the 20 dBm output power was achieved at a reasonable input power level. A Class A topology was used to reduce the complexity of the overall circuit thereby increasing the likelihood that the measured results will correlate with simulations.

B. Amplifier Matching Networks

After the selection of amplifier topology, the input, output and interstage matching networks were developed. First, the input and output impedances of the device were modeled. Using these models, the matching networks were investigated using broadband Q-matching techniques. It will be shown however that the broadband techniques did not

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provide acceptable performance, hence narrowband techniques were used in the final amplifier layout.

Device Input/Output Models

With the input power set at the 1 dB compression point, a load pull analysis was performed on a 300 μm device to find the optimum load for power from 41.5 GHz to 47.5 GHz. This data was then used as a file of reflection coefficients to terminate the output of the device while the input impedance was fitted to an R-C series circuit model. Figure 8 shows the resulting input model for the PHEMT used. The negative inductance does not result from the modeling itself, it is instead a factor inserted afterwards to account for the overestimation of connecting line inductance in the simulations. The value of the negative inductance was provided by Northrop Grumman and is based on measurements.

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PORT    ▣──────────ᄆᲚᲚᲚᲚᲚᲚᲚᲚᲚᲚ ─────────ᄆ   RES
P1                    IND                     R1
port=1                L1                      R=2.91
                      L=-0.07
                                              ᄆ   CAP
                                            ──┴── C1
                                            ───── C=0.58
                                              ᄆ
                                              ⏚
```
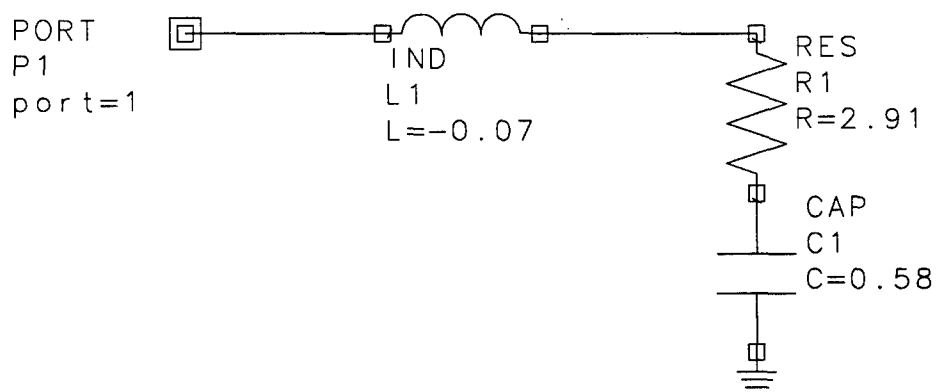
Figure 8: Input model for a 300 μm PHEMT from 41.5 GHz to 47.5 GHz.

The output circuit model topology is based on the approximate model provided in the design manual. The model values were optimized to agree with the conjugate of the optimum load reflection coefficient file. The output model is shown in Figure 9.

7
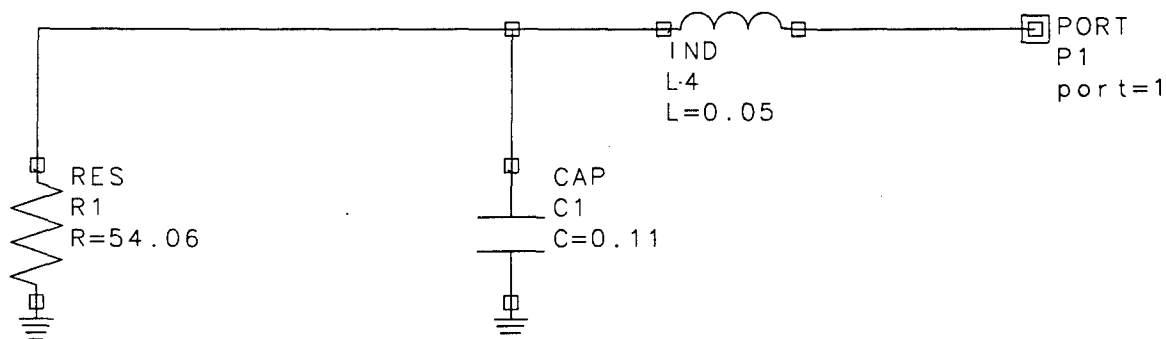
Figure 9: Output model of a 300 μm PHEMT from 41.5 GHz to 47.5 GHz.

Since the optimum load was close to the conjugate match, the outputs of both stages were matched for optimum power to reduce the complexity of the circuit.

Broadband Matching Using Models

Broadband Q-matching was first used in an attempt to design the input, output and interstage matching networks using the device input and output models as terminations. This technique synthesizes a Butterworth response, and the resulting ideal input matching network is shown in Figure 10, with its associated performance in Figure 11. The ideal output matching network schematic is given in Figure 12, with its performance in Figure 13. Figure 14 provides the ideal interstage matching network, while Figure 15 shows the ideal interstage match performance.

Figure 10: Ideal broadband input matching network.

Figure 11: Ideal broadband input match simulations
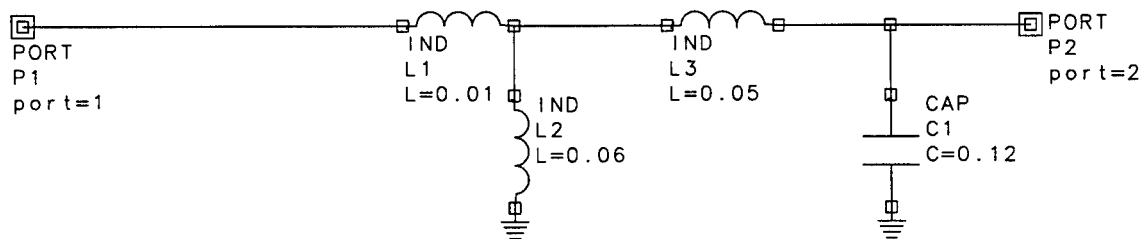
Figure 12: Ideal broadband output matching network.

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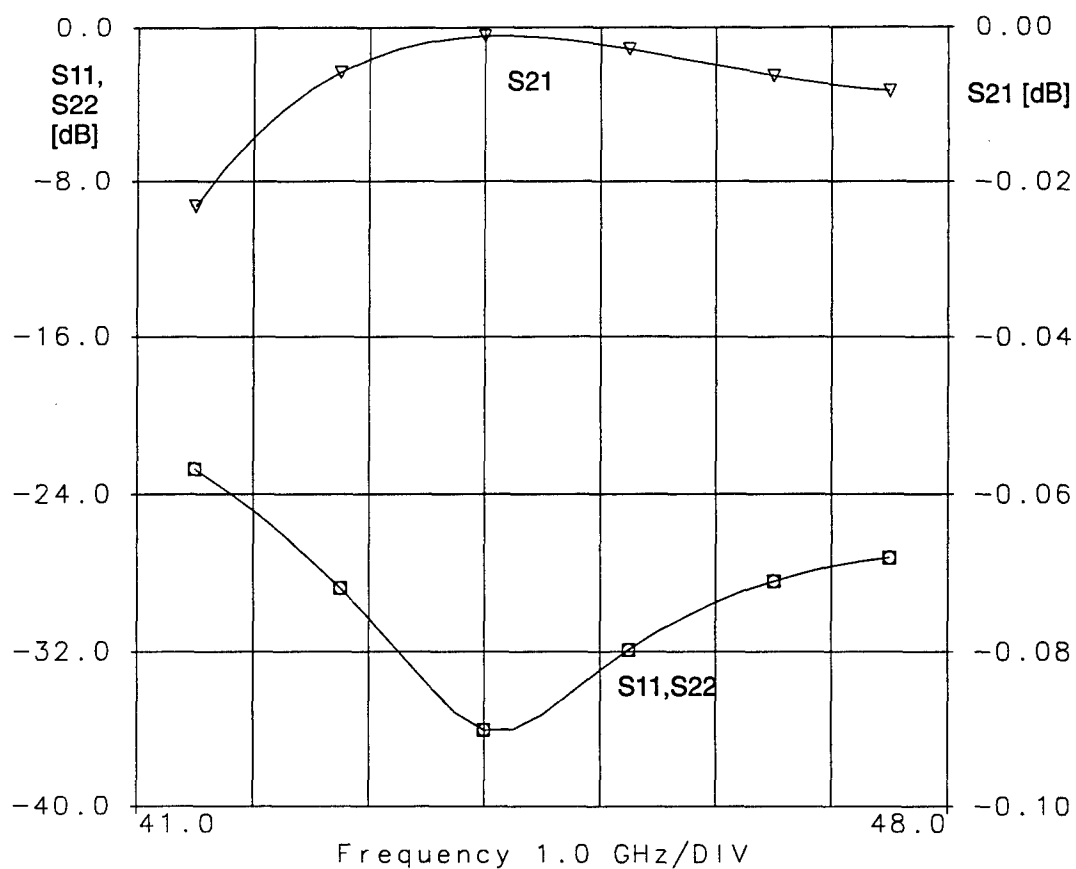
Figure 13: Ideal broadband output match simulation.
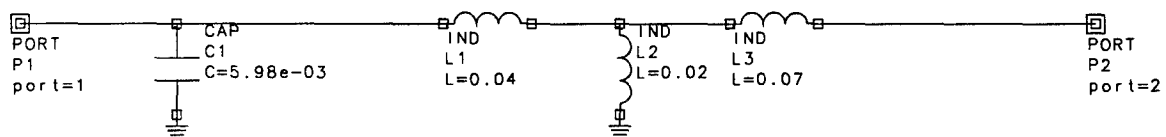
Figure 14: Ideal broadband interstage matching network.
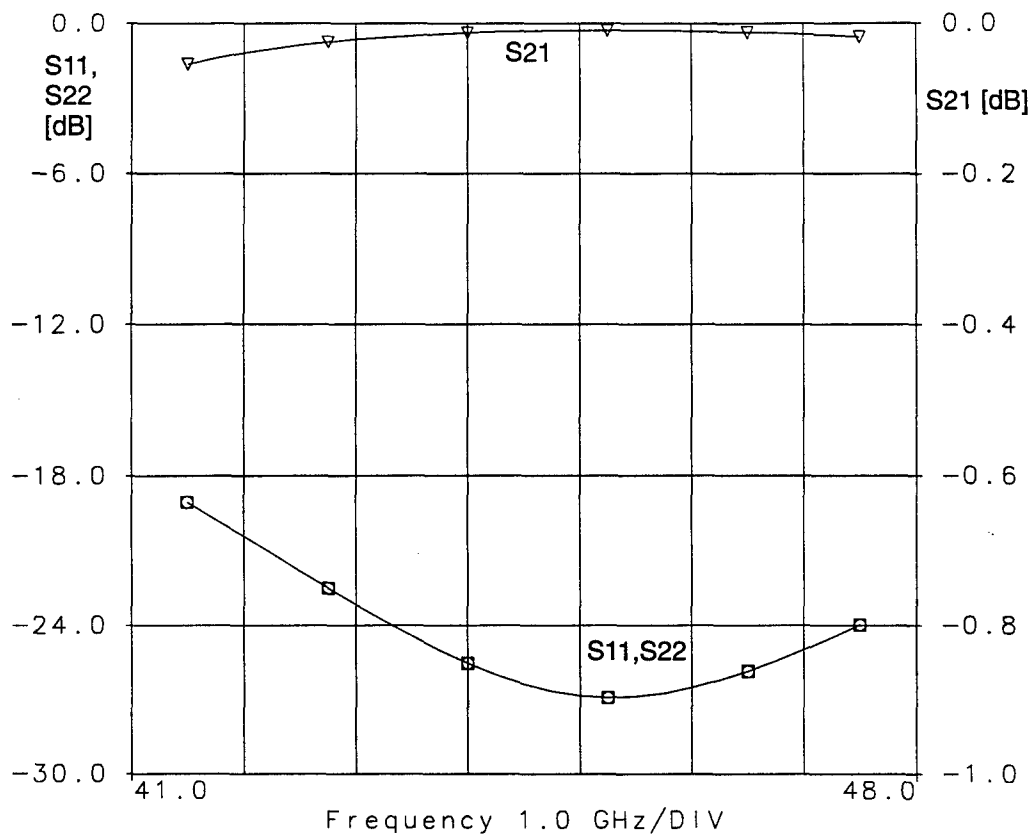
Figure 15: Ideal broadband interstage match simulation.

These broadband networks could not be realized with microstrip elements. The required length of transmission line to enter and leave the device structure was too long and hence gave m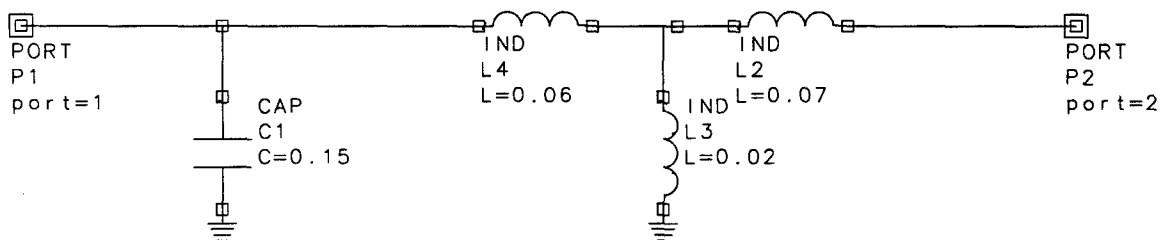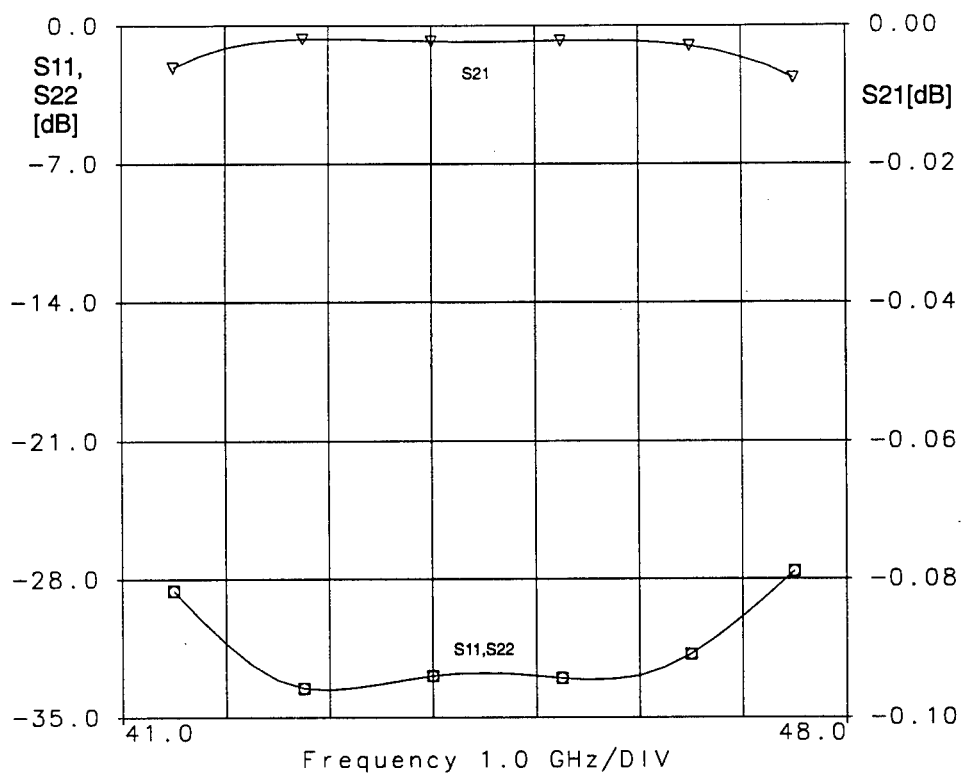ore inductance than could be tolerated by the broadband networks. E-syn™ (a commercial circuit synthesis software package) was used to no avail in an attempt to find other possible broadband topologies. A series capacitor was used to attempt to tune out the additional inductance, however the distributed effect of the capacitor added more inductance, resulting in no improvement. Additionally, a series capacitor was not desirable given the 10 % tolerance of the capacitance and the fact that an exact value was required to resonate with the extra inductance. Coupled lines were also investigated but the distributed inductance nullified the capacitive resonance effect. Therefore, the broadband techniques were abandoned in favour of narrowband techniques.

Narrowband Matching Using Models

The Smith Chart was used to design narrowband matching networks by starting at the input or output model of the device and moving to the 50 Ω reference impedance. For a

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bandpass response giving maximum bandwidth it is desired to alternate between low-pass elements and high-pass elements. Bandwidth is also maximized by staying within the Q-circle of the termination with the larger Q. Unfortunately the high-low element approach conflicts with the Q-circle condition if realizable transmission line element values are used, e.g. the minimum lengths required to connect to the device itself. This conflict confirmed why the broadband approach failed. It was decided to use only low-pass elements as they give a more realizable topology while staying within the necessary Q-circle to extend the bandwidth of the match.

Therefore, using the input model as a starting point, ideal low-pass transmission line elements were used to move across the Smith Chart to form the match. The resulting input match is shown in Figure 16; note that the input model Q circle of 2.13 is not exceeded. The same procedure was used, with the output model as a starting point, to develop the output match, and the resulting Smith Chart is shown in Figure 17. Again the output model Q of 1.6 was not exceeded, and low pass elements were used.

The electrical lengths of the ideal transmission lines were then used to determine the physical lengths of the microstrip transmission lines. Crosses and tees were also added, as were step discontinuities. The microstrip lines were all selected to be 50 Ω, except close to the input of the device where a narrower 25 μm line was required because of the proximity of the source via holes. Figure 18 shows the final input matching circuit with microstrip elements after optimization, and Figure 19 gives the simulated performance with the input model as a termination. Note that in Figure 18 the line between the two stubs was shortened and then removed during the optimization phase.
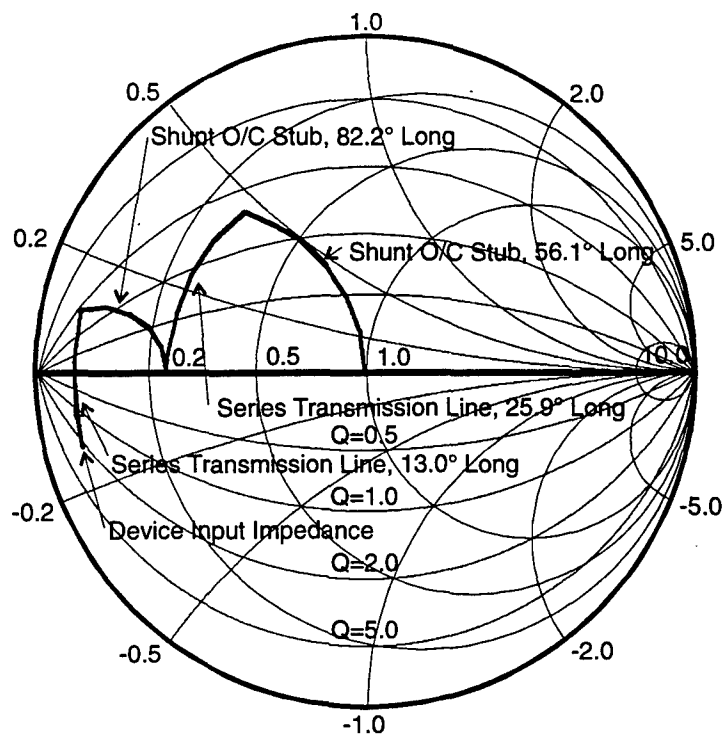
Figure 16: Smith Chart of input match using ideal elements.
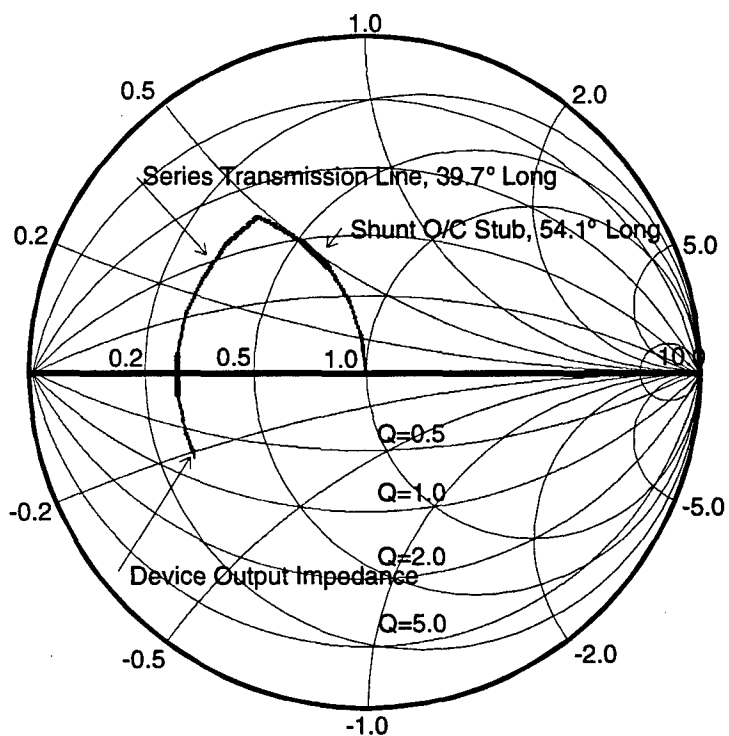
Figure 17: Smith Chart of output match using ideal elements.

13
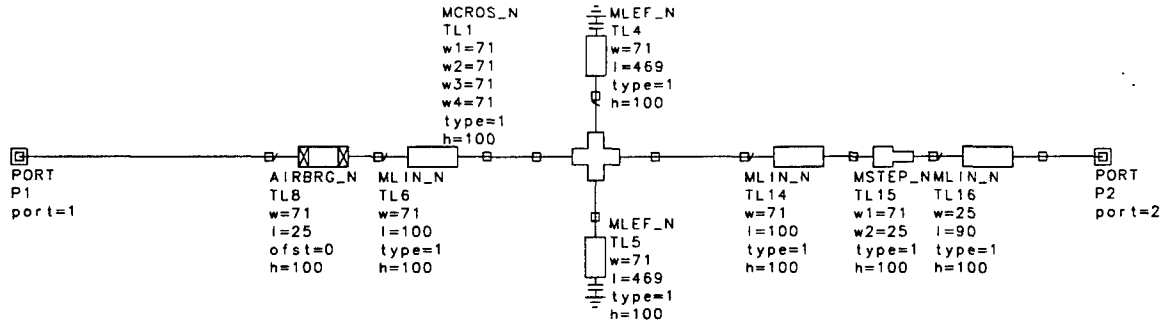
Figure 18: Input matching network with microstrip elements after optimization.
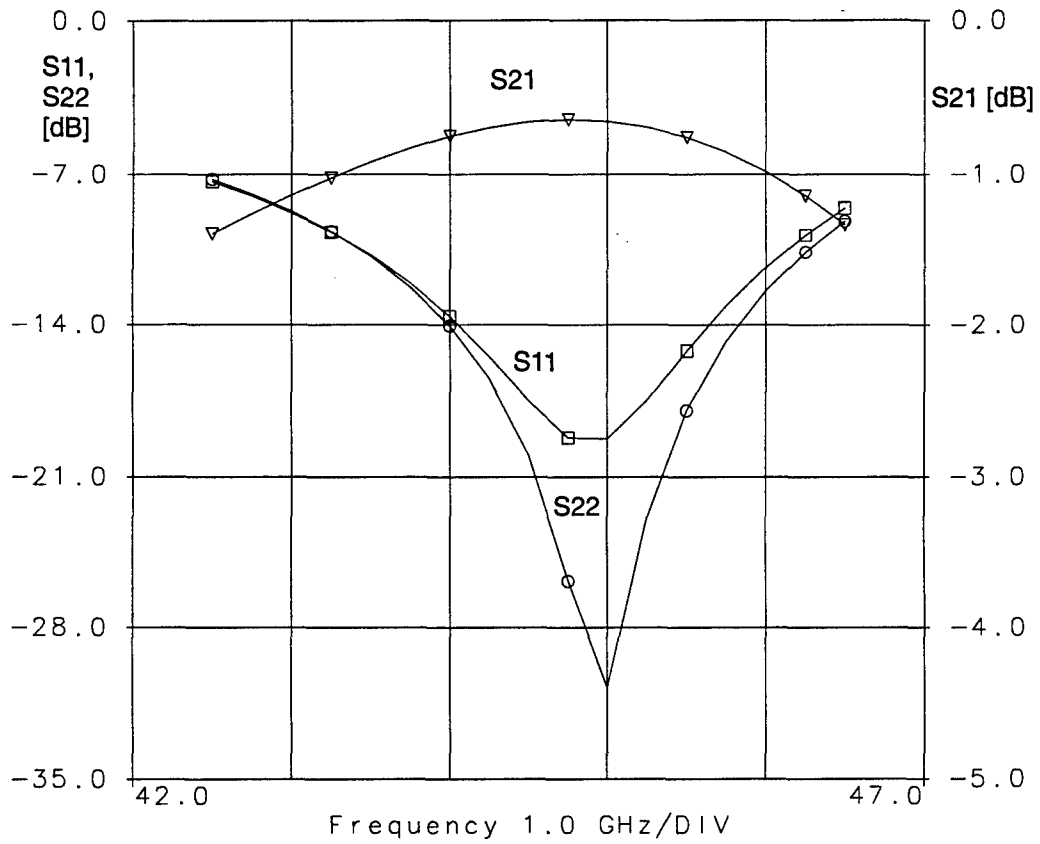
Figure 19: Input matching network performance with optimized microstrip elements and input model termination.

The final output matching circuit after optimization is provided in Figure 20. The simulated performance of the output matching circuit with the output model as a termination is given in Figure 21.

14
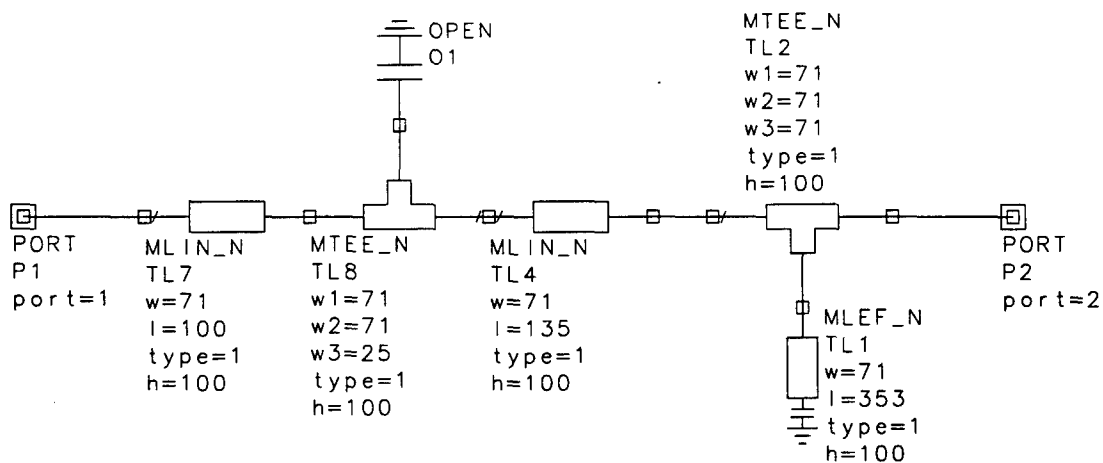
Figure 20: Output matching network with microstrip elements.
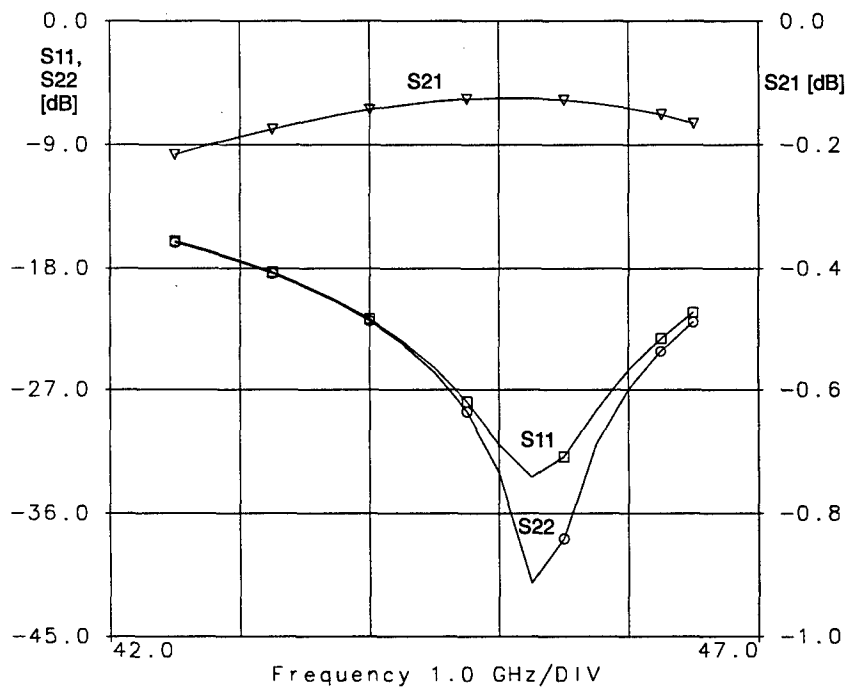
Figure 21: Output matching network performance with microstrip elements and output model termination.

The interstage matching network was also addressed using the Smith Chart approach, however the resulting network was not realizable. The transmission line lengths were not long enough to provide adequate spacing between the devices. Additionally, the distributed effect from a dc blocking capacitor would force the transmission lines lengths to be further modified. It was decided to use the existing input and output matching networks and match

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the interstage to an interim value of 50 Ω. This significantly reduces the effect of the dc blocking capacitor, as the distributed effects are minimal if a 50 Ω transmission line is used for the capacitor plates within a 50 Ω system at that point. A 71 x 71 μm capacitor exactly fits within the width of a 50 Ω transmission line (C = 1.84 pF) and the 10% capacitance variation will not significantly affect the impedance or, by extension, the interstage match. The trade-off to this approach is the extra space required. However the performance improvement justified the extra space.

The interstage matching network, as realized in microstrip, is shown in Figure 22 without the dc blocking capacitor. The simulated performance with the input and output models as terminations is given in Figure 23.
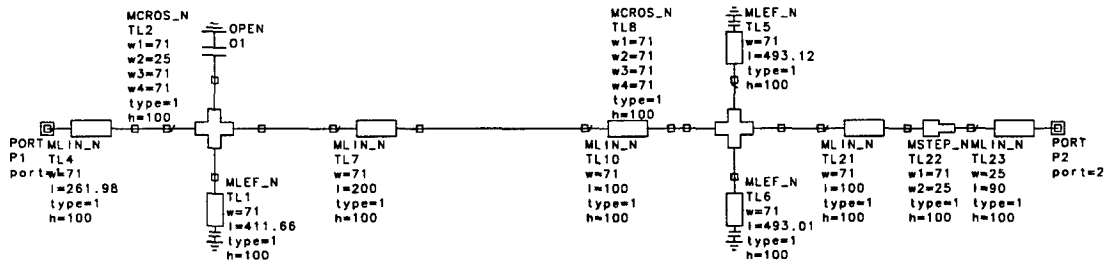
Figure 22: Interstage matching network in microstrip (dc blocking capacitor is assumed to be transparent).
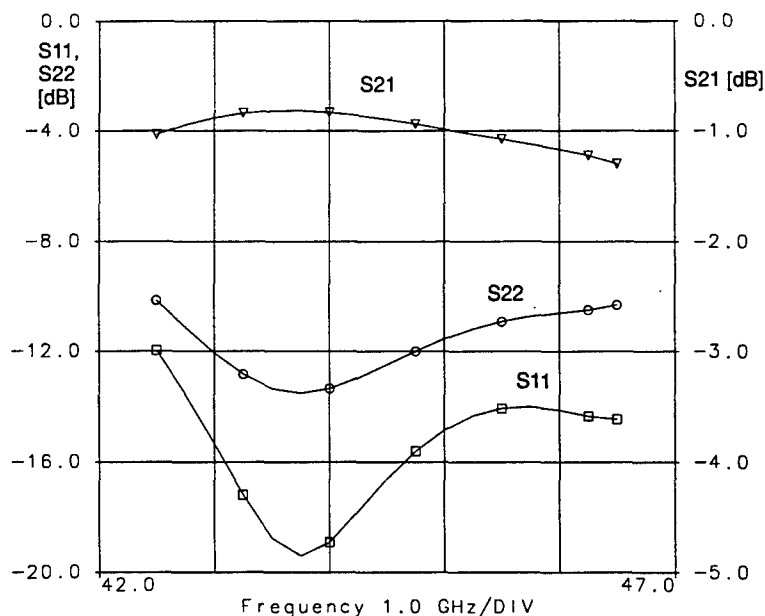
Figure 23: Interstage matching network performance with microstrip elements and with the input and output models as terminations.

C. Bias Networks, Chokes and DC Blocking Capacitors

Quarter wavelength microstrip transmission lines were used as the bias chokes. Large capacitors provided an RF short circuit, while blocking the dc from entering the via hole. The chokes were not bent to increase the accuracy of the simulations.

DC blocking capacitors were added at the input and the output. These capacitors were not included in the input or output matching networks to minimize the affect on overall performance.

The interstage dc blocking capacitor was also placed to minimize its affect on the match by placing it in a region close to 50 Ω where the frequency dependence of the distributed effects is lowered.

The blocking capacitors were used where possible to bring in the dc bias. This avoids using more tee junctions than absolutely necessary.

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D. Amplifier Small Signal Performance

The resulting matching networks, blocking capacitors, chokes and bias circuitry were then used in conjunction with the actual non-linear device models to simulate performance. The input, output and interstage matching networks were optimized for gain compensation, input and output match. The final simulated input and output match for the two-stage amplifier is given in Figure 24. The final small signal gain of the two-stage amplifier is shown in Figure 25.
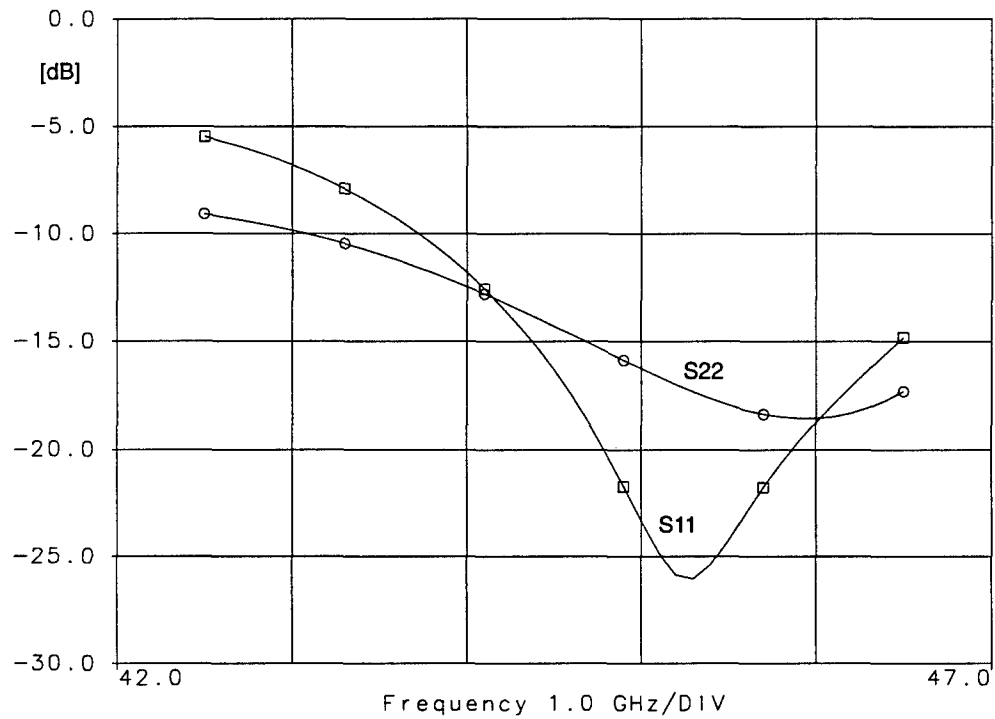
Figure 24: Input and output match of the two-stage amplifier.
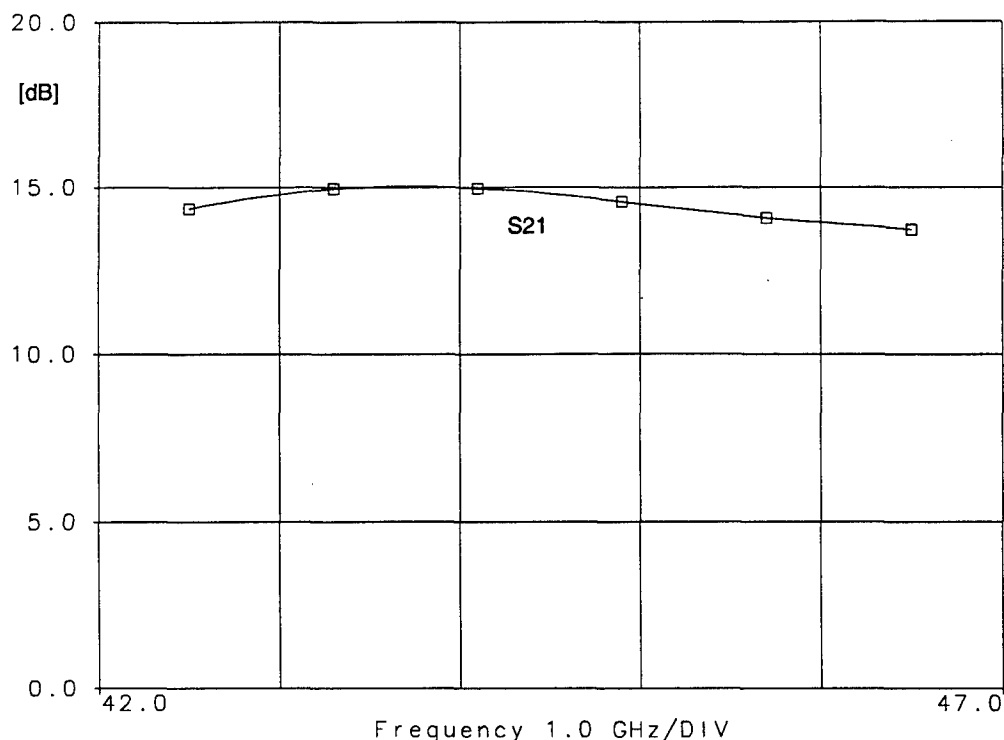
Figure 25: Small signal gain of the two-stage amplifier.

E. Amplifier Stability

The two-stage amplifier was found to be stable within the desired bandwidth of 43.5 GHz to 45.5 GHz, but unstable from 7 GHz to 22 GHz. The out-of-band instability was addressed by adding resistors behind the drain chokes of the two devices. This had the effect of loading the transistors out-of-band thereby reducing the gain and increasing stability. The resistors were added before the RF shorting capacitor since the drain current is quite large and a resistor in the dc path would have reduced the dc bias voltage. The degradation in the RF short due to the presence of this resistor was tolerable. Additionally, the RF shorting capacitors were reduced in size to exactly resonate with the via hole inductance. This provided narrowerband short in the band of interest and hence further loaded the devices out of the band of interest. It should be noted that the value of the capacitor could change with the manufacturing tolerances. However, the increase in stability was worth the trade-off. Furthermore, the via hole capacitor resonance is not very sharp so capacitance variations should be tolerable. The stability of the final two-stage amplifier is shown in Figure 26.

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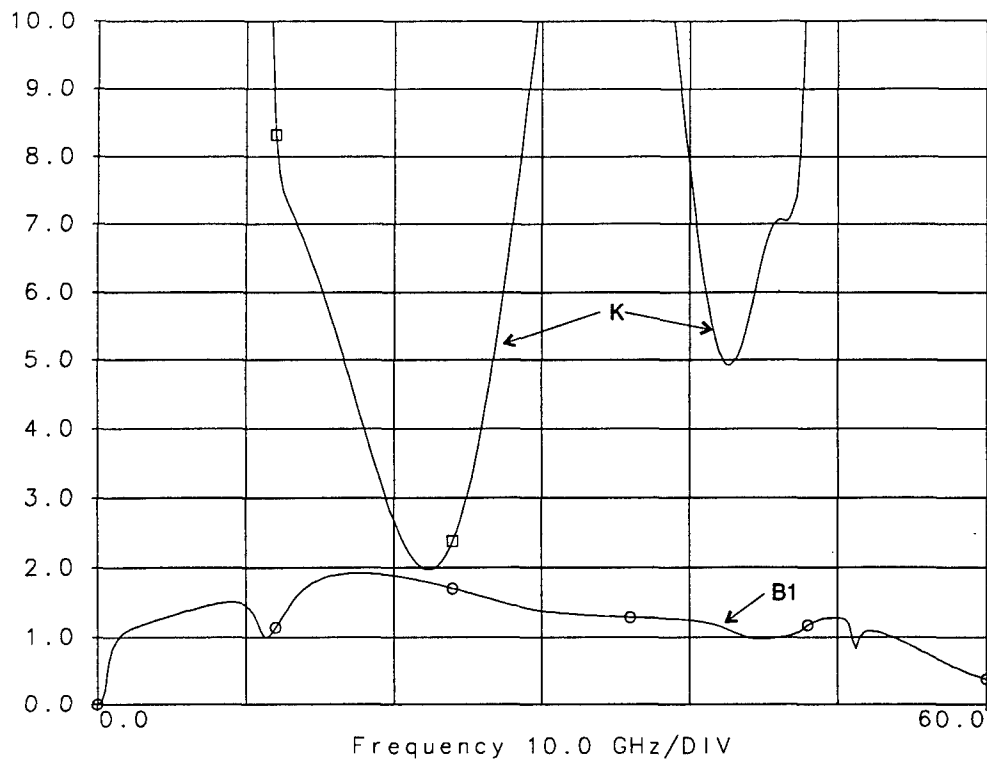
Figure 26: Amplifier Stability.

F. Amplifier Schematics

The final simulated schematic of the two stage amplifier is shown in Figure 27. The final input, interstage and output matching network schematics with bias, chokes, stabilizing resistors and blocking capacitors, are shown in Figures 28, 29 and 30 respectively.
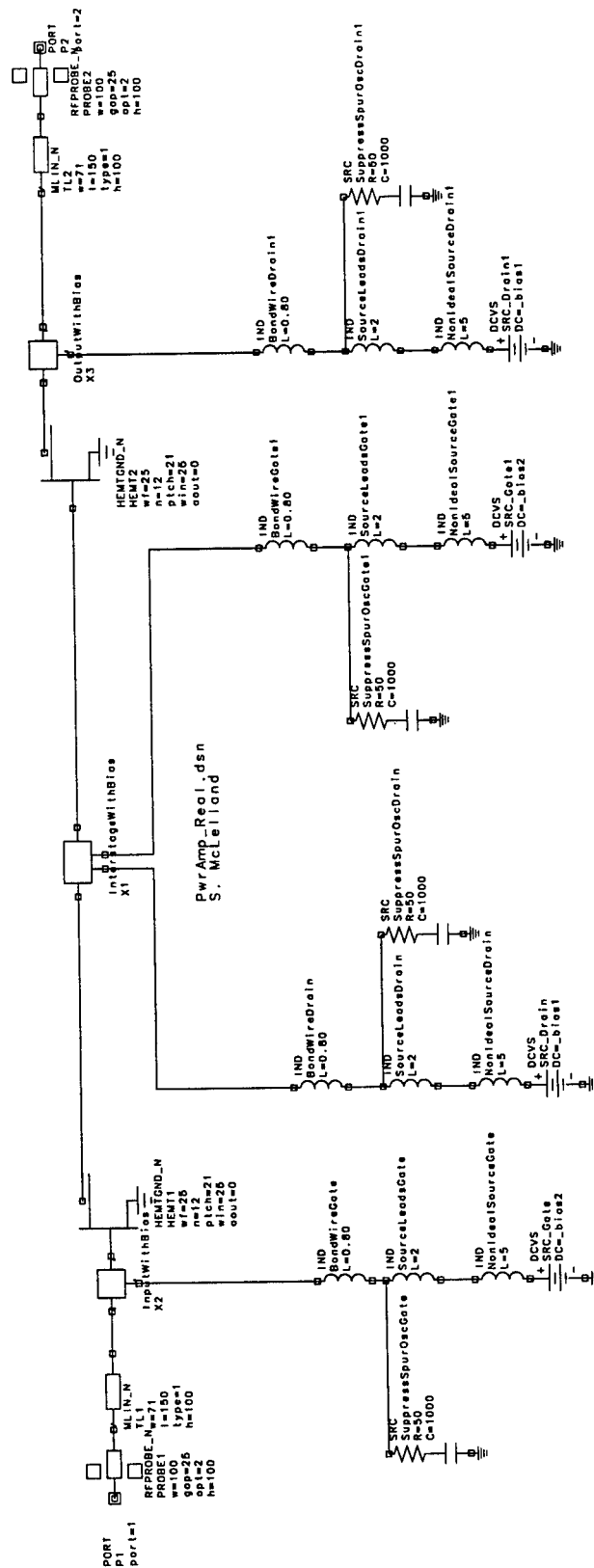
Figure 27: Final two stage amplifier schematic.

PORT
P3
port=3

BPAD_N
TL3
w=100
l=100
h=100

MLIN_N
TL19
w=25
l=200
type=1
h=100

AIRBRG_N
TL10
w=25
l=15
ofst=0
h=100

CAP2T_N
C2
w=47
l=47
h=100

VIA1_N
VIA2
w=100

AIRBRG_N
TL9
w=25
l=15
ofst=0
h=100

MLIN_N
TL13
w=25
l=574
type=1
h=100

AIRBRG_N
TL7
w=25
l=15
ofst=0
h=100

MCROS_N
TL1
w1=71
w2=71
w3=71
w4=71
type=1
h=100

MLEF_N
TL4
w=71
l=437
type=1
h=100

PORT   MLIN_N
P1   TL2
port=1   w=71
              l=100
              type=1
              h=100

CAP2L_N
C1
w=71
l=71
h=100

AIRBRG_N
TL8
w=71
l=25
ofst=0
h=100

MLIN_N
TL6
w=71
l=100
type=1
h=100

MLEF_N
TL5
w=71
l=458
type=1
h=100

MLIN_N
TL14
w=71
l=100
type=1
h=100

MSTEP_N
TL15
w1=71
w2=25
type=1
h=100

MLIN_N
TL16
w=25
l=90
type=1
h=100

PORT
P2
port=2

InputWithBias.dsn
S. McLeiland

Figure 28: Final input matching network schematic.

Figure 29: Final interstage matching network schematic.
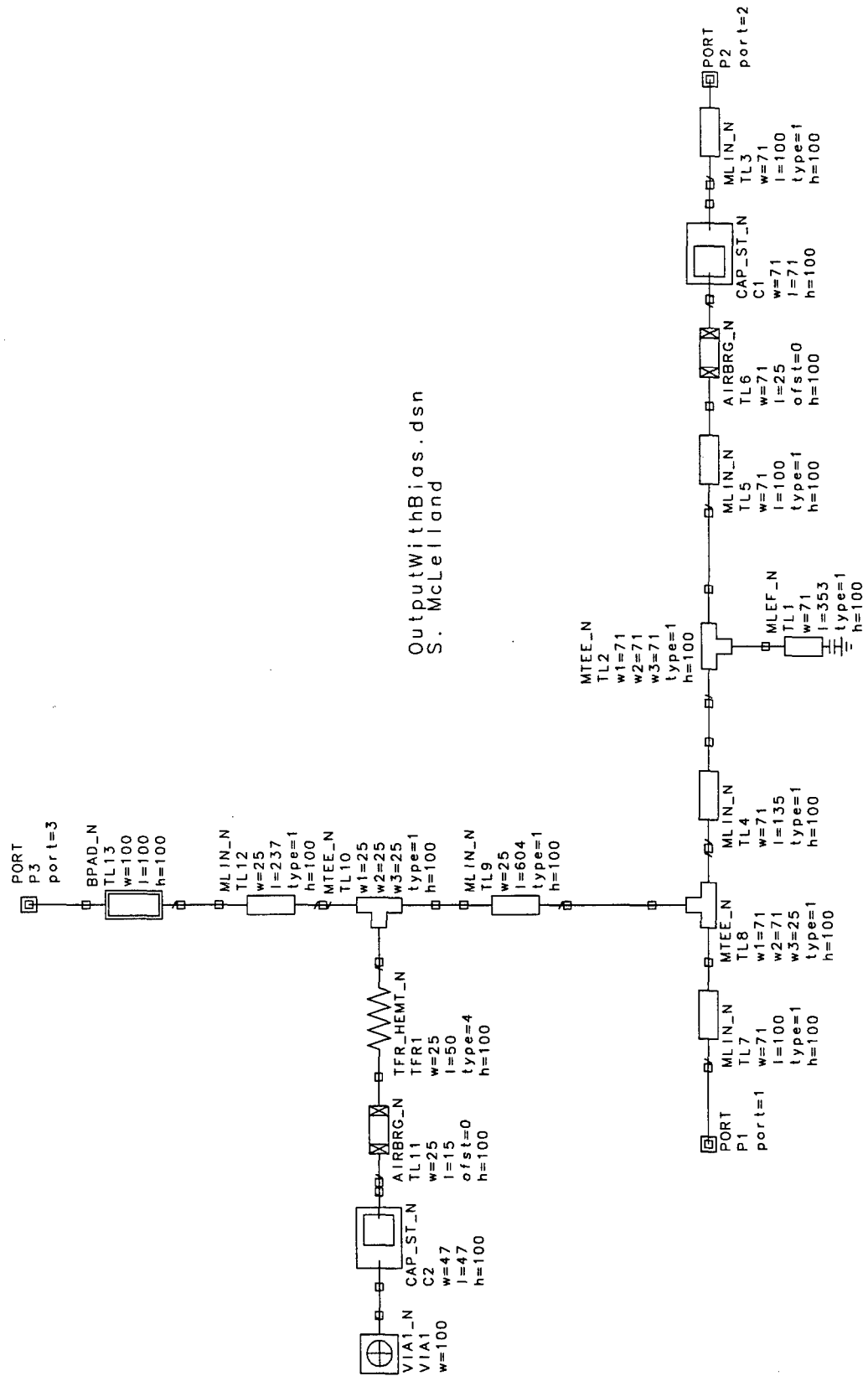
Figure 30: **Final output matching network schematic.**
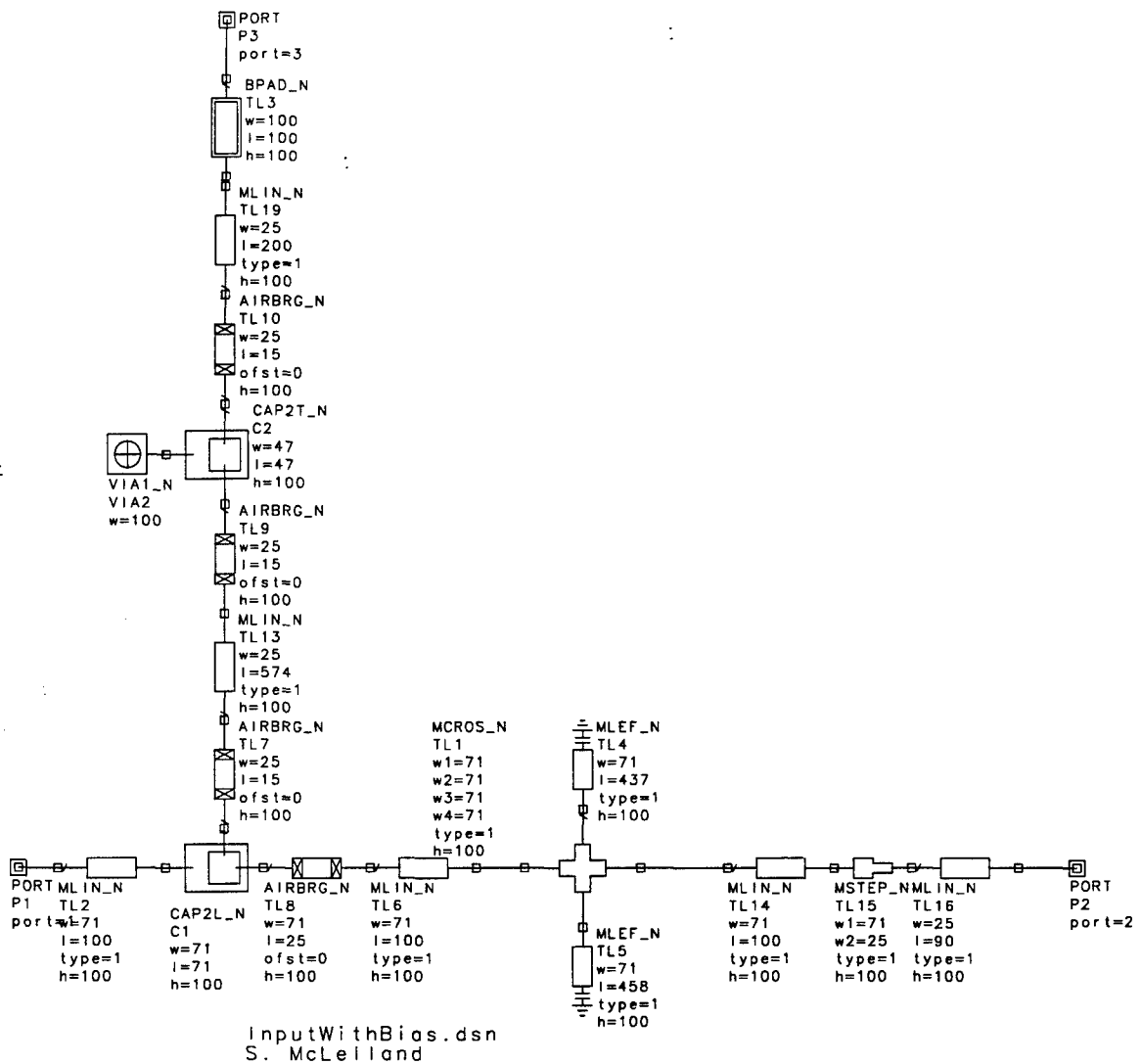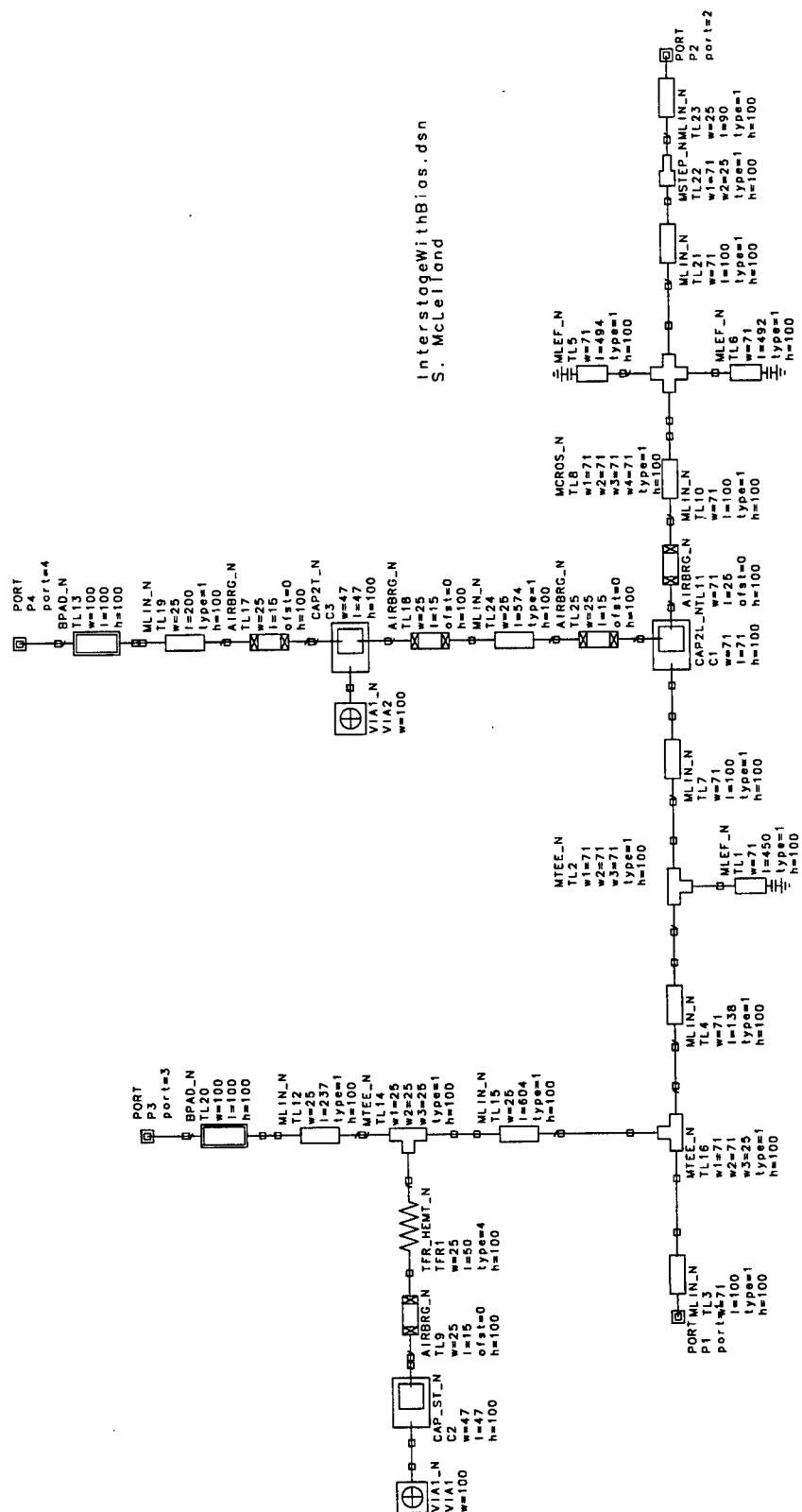
G. Amplifier Large Signal Performance

The amplifier was simulated using harmonic balance to analyze its large signal behavior. The resulting P_{out} versus P_{in} curves are shown in Figure 31. For 20 dBm output power, the input power and gain as a function of frequency is provided in table 1.
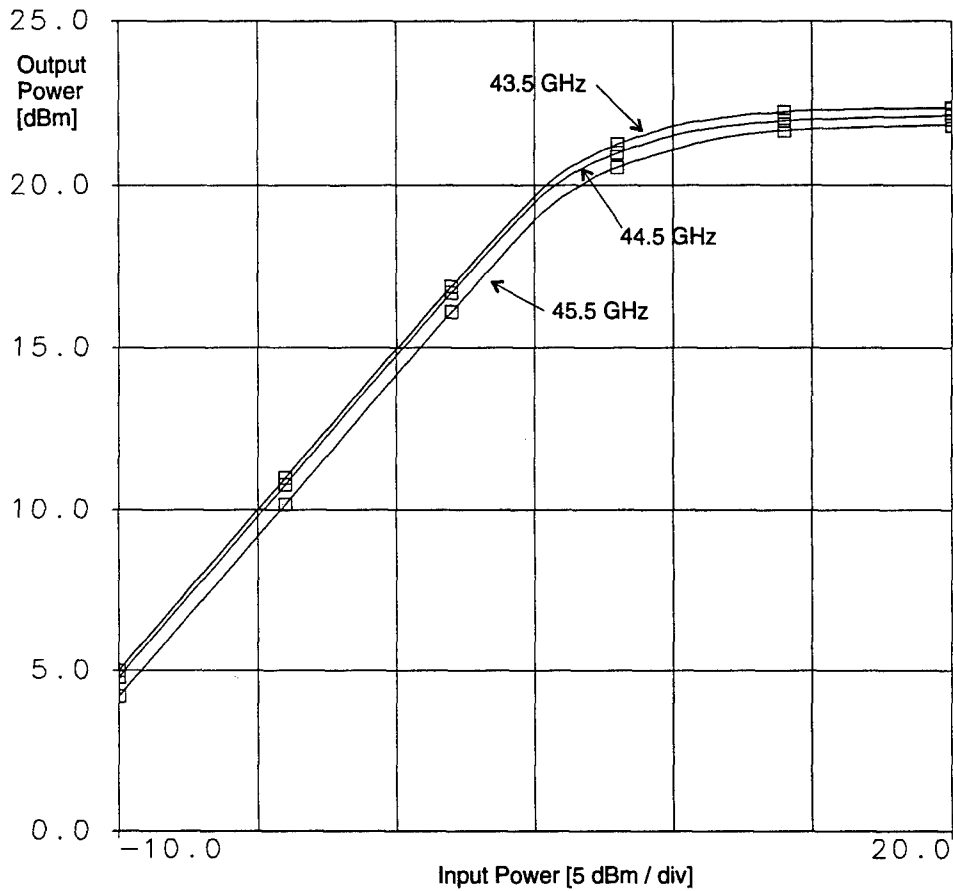
Figure 31: Output power as a function of input power over the desired bandwidth.

Table 1: Large signal performance of the two stage amplifier as a function of frequency.

Frequency [GHz]	Input Power [dBm]	Output Power [dBm]	Gain
42.5	8.00	20.61	12.61
43.5	8.00	20.60	12.60
44.5	8.00	20.35	12.35
45.5	8.00	20.01	12.01
46.5	8.00	19.56	11.56

H. Electromagnetic Simulations

Critical sections of the amplifier were analyzed using the SONNET™ electromagnetic simulator. Specifically, the following sections were examined:

- the entire input matching network
- the entire output matching network
- the entire interstage matching network
- all dc blocking capacitors
- the quarter wavelength chokes
- the resistor-capacitor stabilization network

All coupling of transmission lines within these sections was accounted for. However coupling between these sections was not considered due to time and memory constraints. The via holes were not analyzed for the same reasons.

The substrate for the microstrip lines was GaAs only. The substrate for the capacitors consisted of GaAs, a layer of Si_3N_4, and a layer of air for the air bridges. The minimum cell size used was 5 μm^2 in all cases.

The matching networks were optimized using SONNET™. The resulting amplifier small signal performance is shown in Figures 32 and 33. The EM optimized large signal performance is given in Figure 34 and Table 2.

The critical sections were also analyzed from 1 GHz to 60 GHz to check stability, and these results are presented in Figure 35.
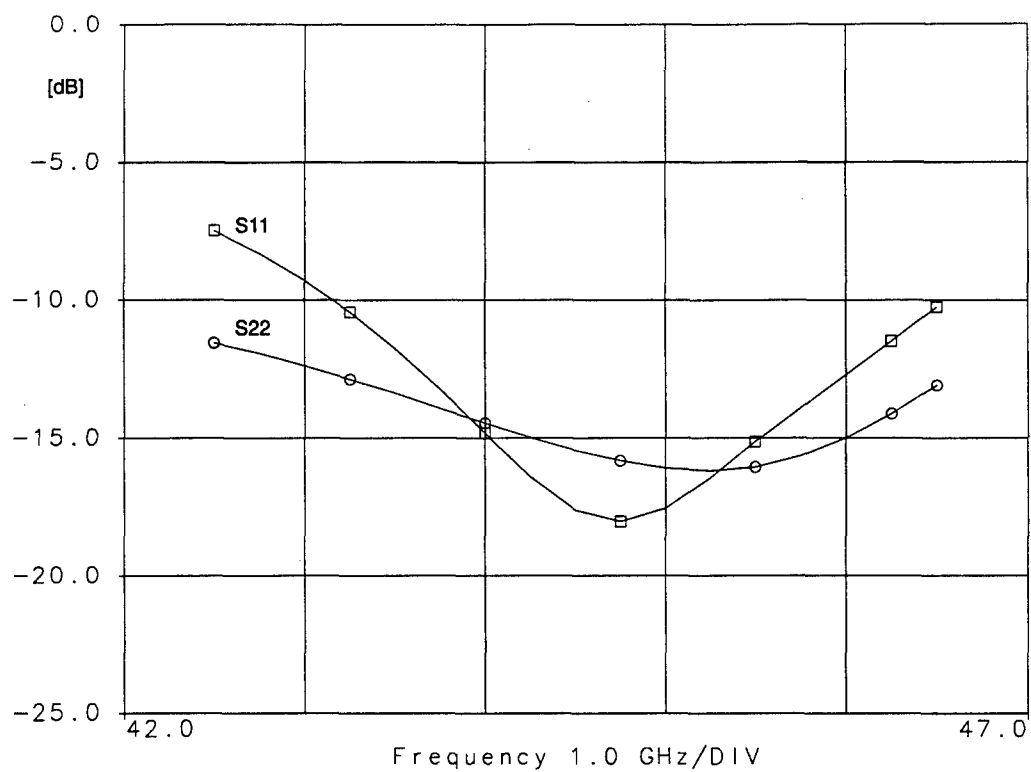
Figure 32: EM simulated amplifier performance after optimization.
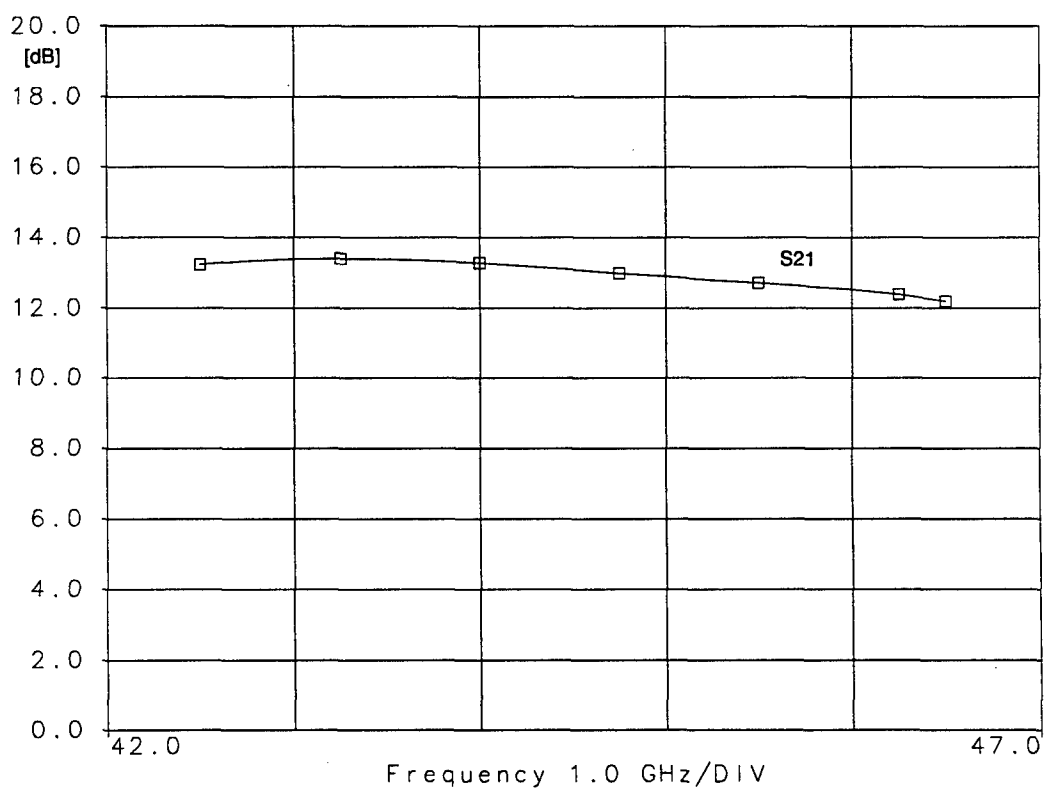
Figure 33: EM simulated amplifier performance after optimization.

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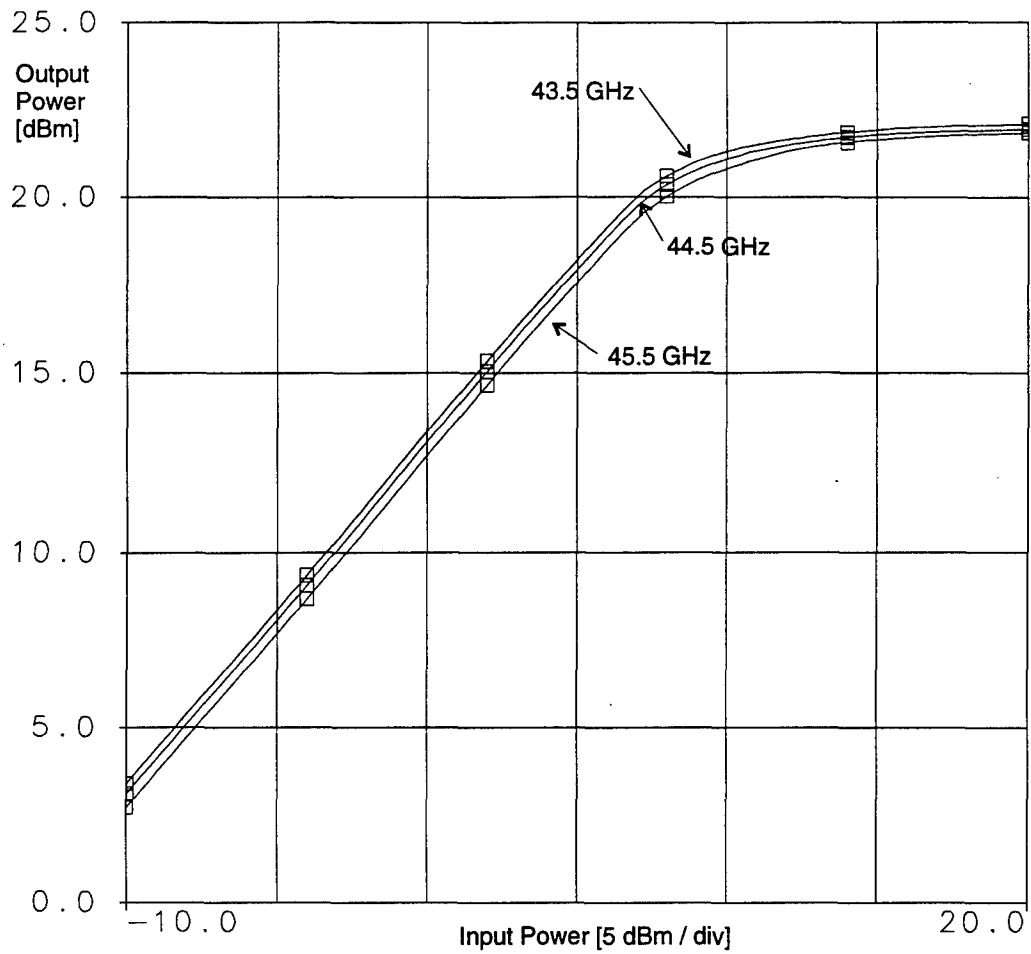
Figure 34: Amplifier large signal performance after EM optimization.

Table 2: Large signal performance of the two stage amplifier as a function of frequency after EM optimization.

Frequency [GHz]	Input Power [dBm]	Output Power [dBm]	Gain
42.5	8.00	20.61	12.61
43.5	8.00	20.60	12.60
44.5	8.00	20.35	12.35
45.5	8.00	20.01	12.01
46.5	8.00	19.56	11.56

Figure 35: Amplifier stability from EM analysis.

I. Amplifier Layout

Using the results from the electromagnetic optimization a final layout for the two stage amplifier was realized and is shown in Figure 36.
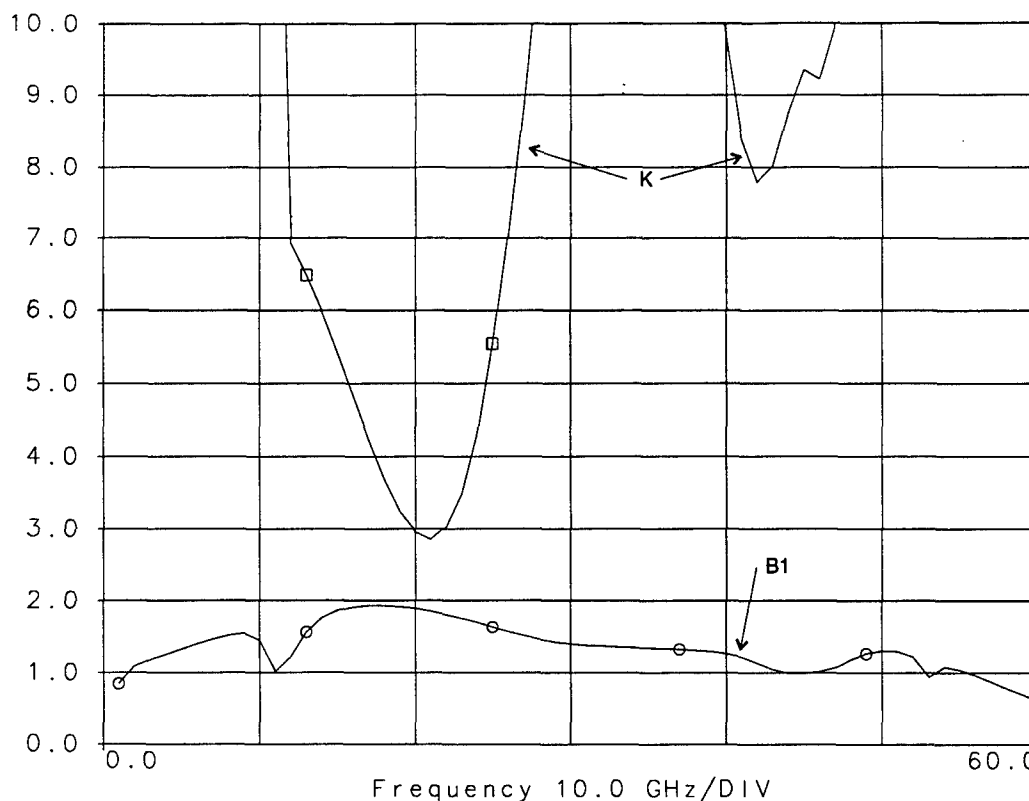
J. Amplifier With Interconnects

The amplifier was altered slightly to account for bond wire interconnects. The stub lengths were optimized to reduce the performance degradation due to the bond wire inductances. Figures 37 and 38 show the simulated small signal performance with bond wire inductances of 0.15 nH. Figure 39 gives the large signal amplifier performance with interconnects and the simulated stability is shown in Figure 40. All results are from electromagnetic simulations. A final layout for the amplifier with interconnects is provided in Figure 41.

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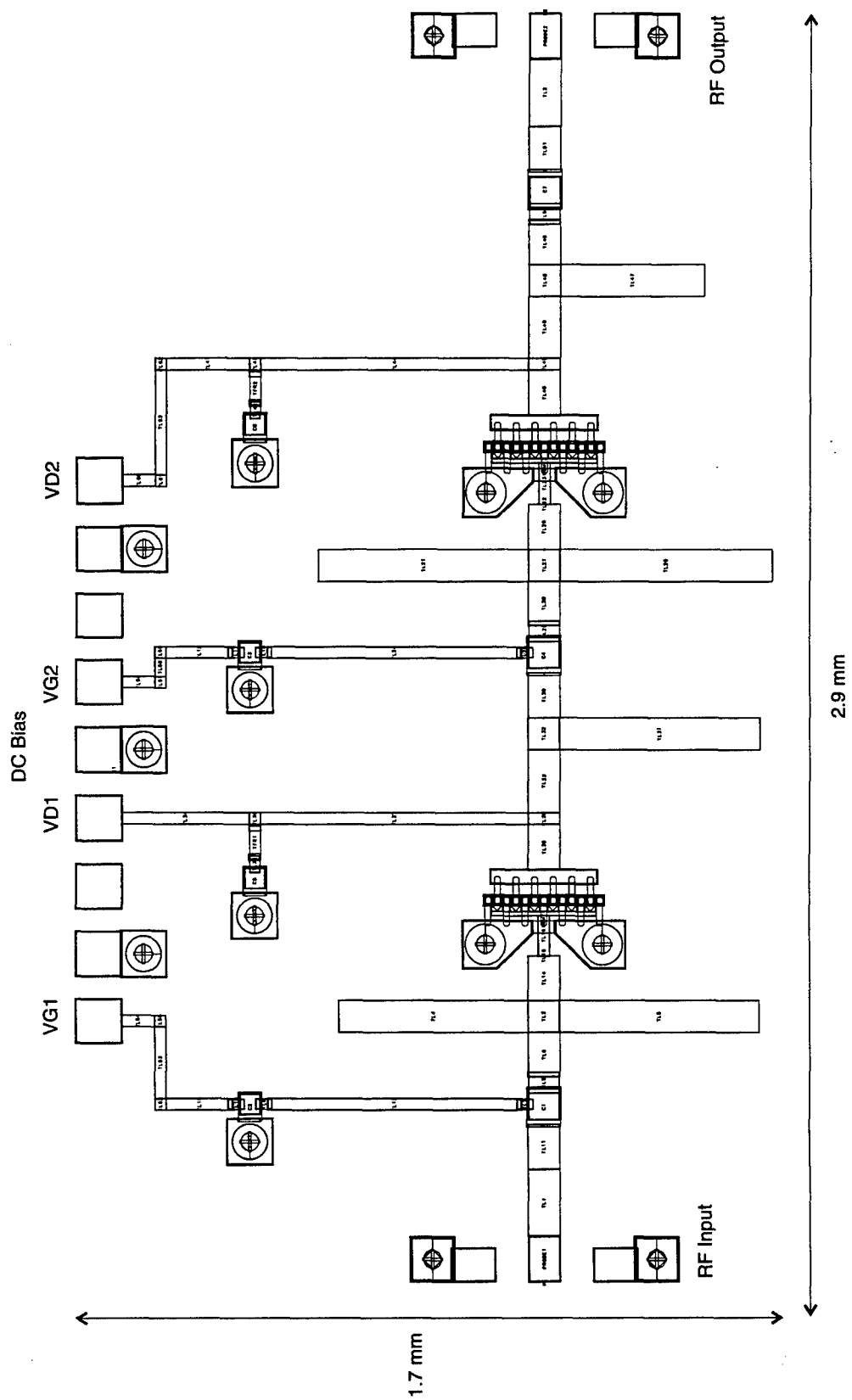
Figure 36: **Final two stage amplifier layout.**
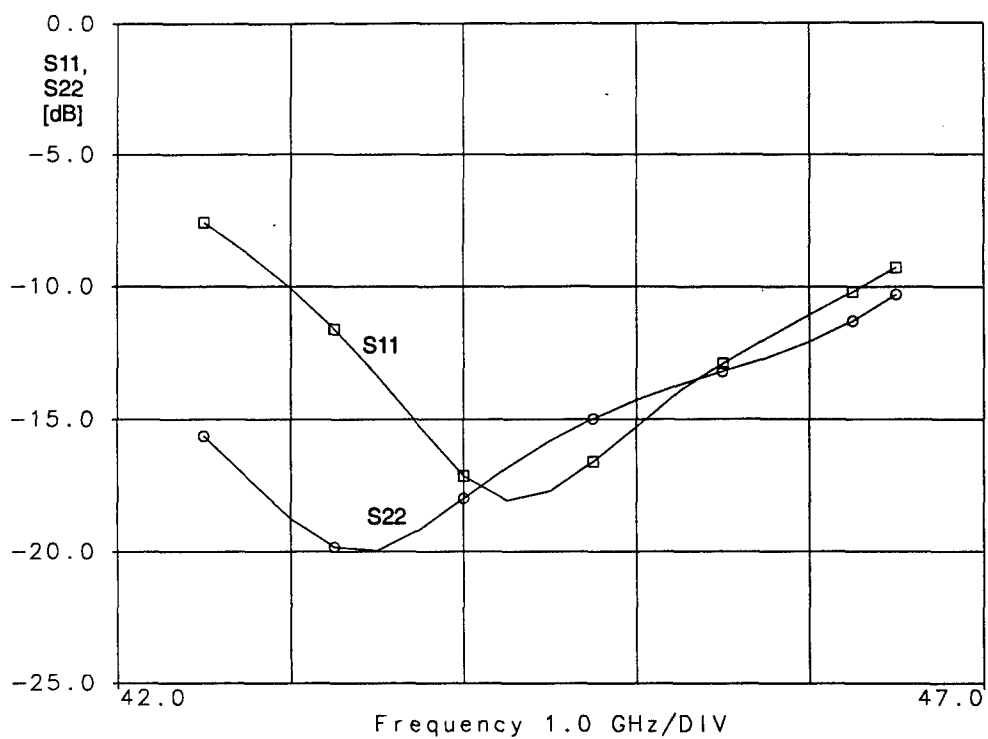
Figure 37: Small signal return loss performance of the amplifier with interconnects (after EM optimization).
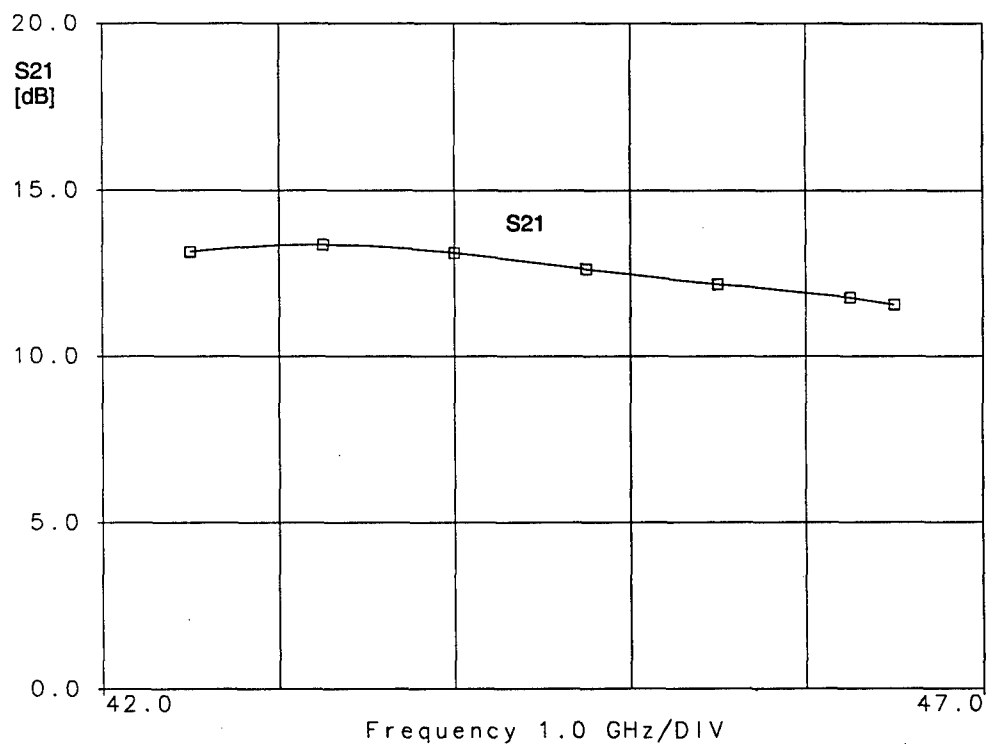
Figure 38: Small signal gain performance of the amplifier with interconnects (after EM optimization).

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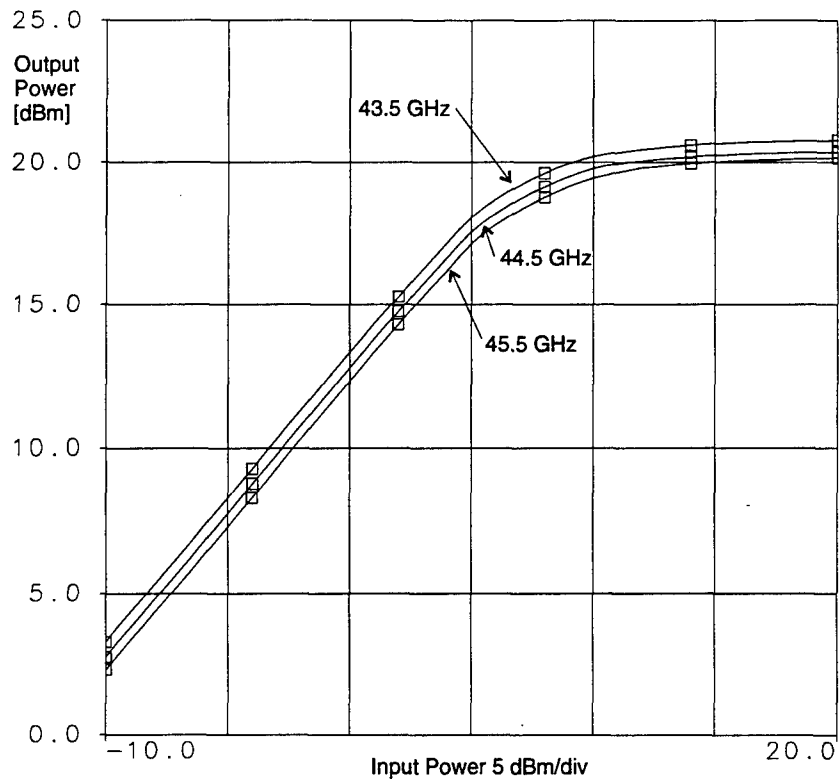
Figure 39: Large signal saturation performance of the amplifier with interconnects (after EM optimization).
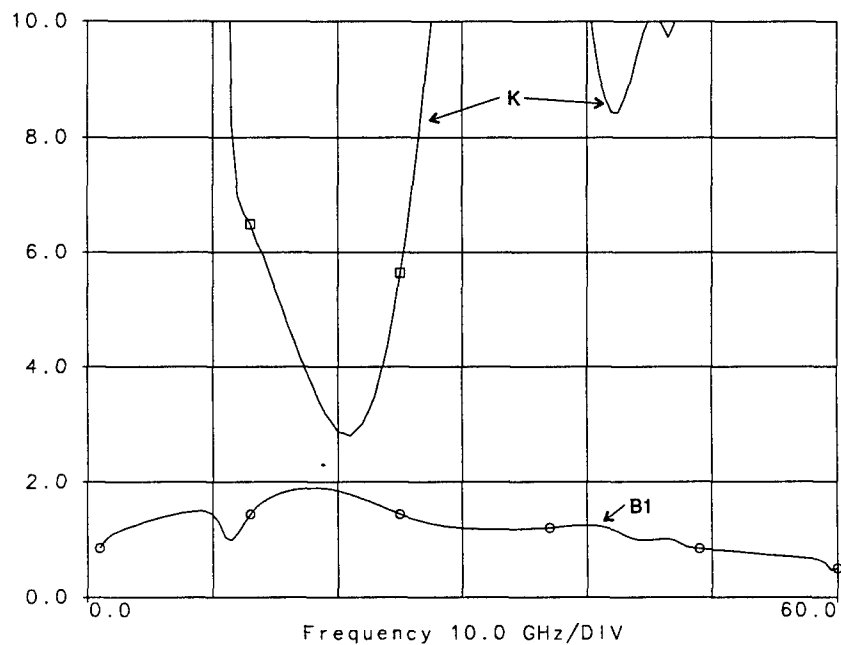
Figure 40: Stability of the amplifier with interconnects (after EM optimization).

Figure 41: Final layout of the amplifier with interconnects.

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Dual Amplifier Chain Performance

The performance of two amplifiers connected in series was briefly investigated. The amplifiers modified for interconnects were used and the resulting EM simulated small signal performance is shown in Figures 42 and 43.
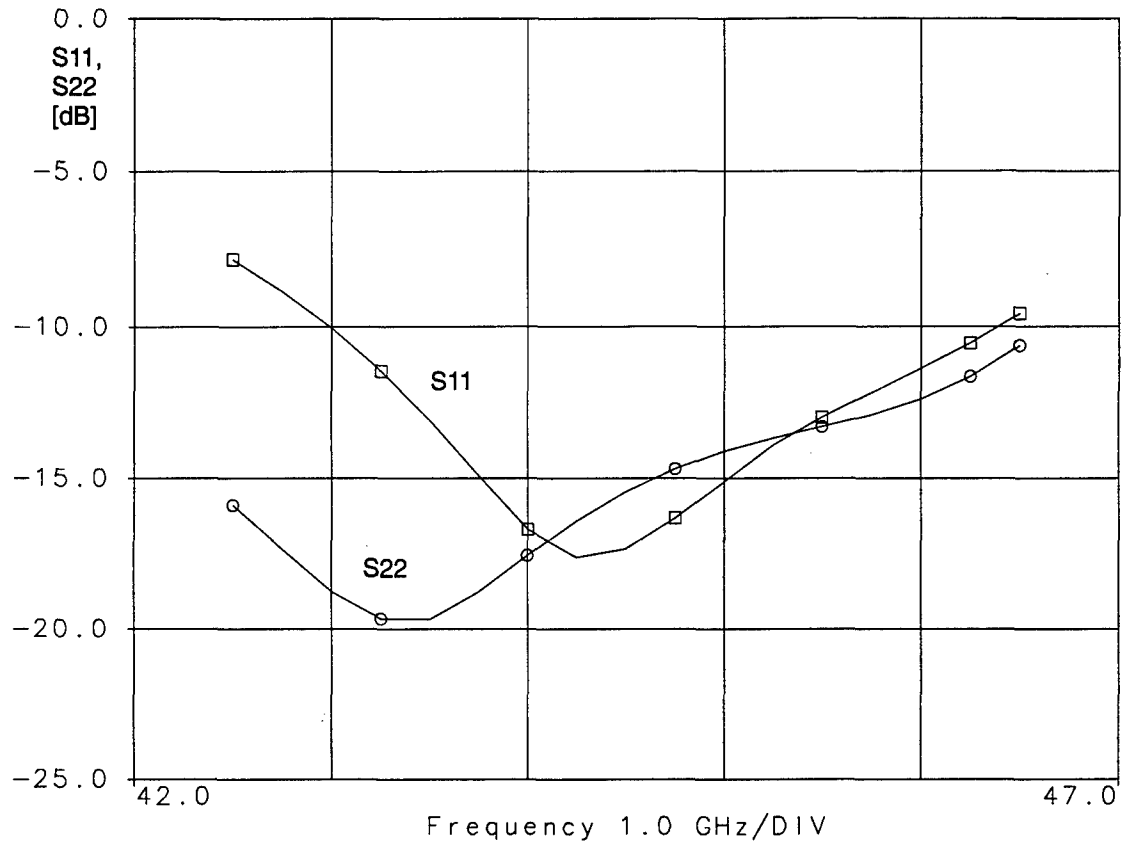
Figure 42: Small signal return loss performance of two amplifier chain with interconnects.
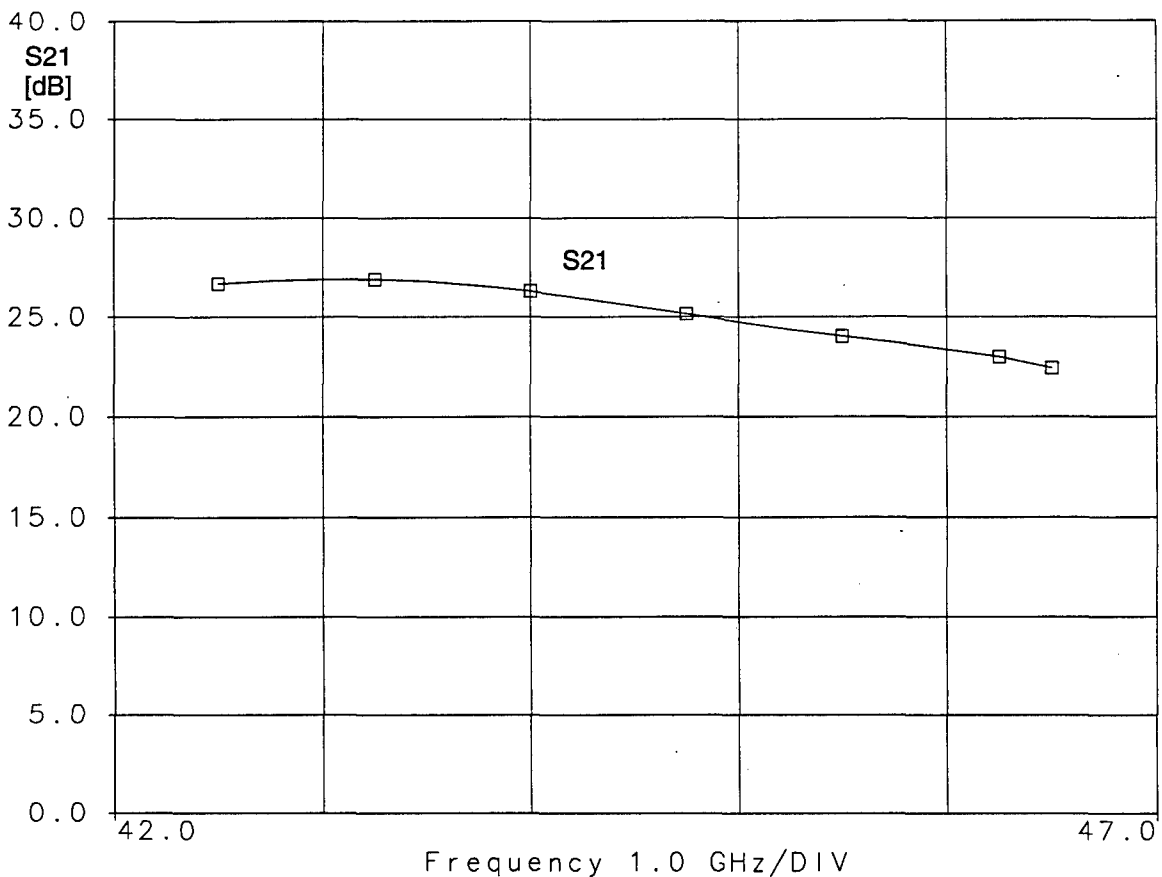
Figure 43: Small signal gain performance of two amplifier chain with interconnects.

III. Summary and Conclusions

The design procedure of a 44 GHz PHEMT power amplifier in GaAs MMIC technology was presented. The chip is expected to provide 100 mW output power over the frequency range 43.5 - 45.5 GHz. The chip has 12 dB gain and the predicted input and output return loss characteristics will allow it to be cascaded if more gain is required.

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The work described in this report represents the design phase of a gallium arsenide monolithic microwave integrated circuit (GaAs MMIC) power amplifier using pseudomorphic high electron mobility transistors (PHEMTs). The main purpose was to investigate the possible performance of a power amplifier at 44 GHz for future application in a phased array antenna system. The design of a two stage amplifier, providing over 12 dB of gain over the frequency range 43.5 - 45.5 GHz, is described along with the expected large signal performance. It is expected that the amplifier will provide over 20 dBm of output power. The final layout of the complete chip is also presented.

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mmic, sspa, power amplifier